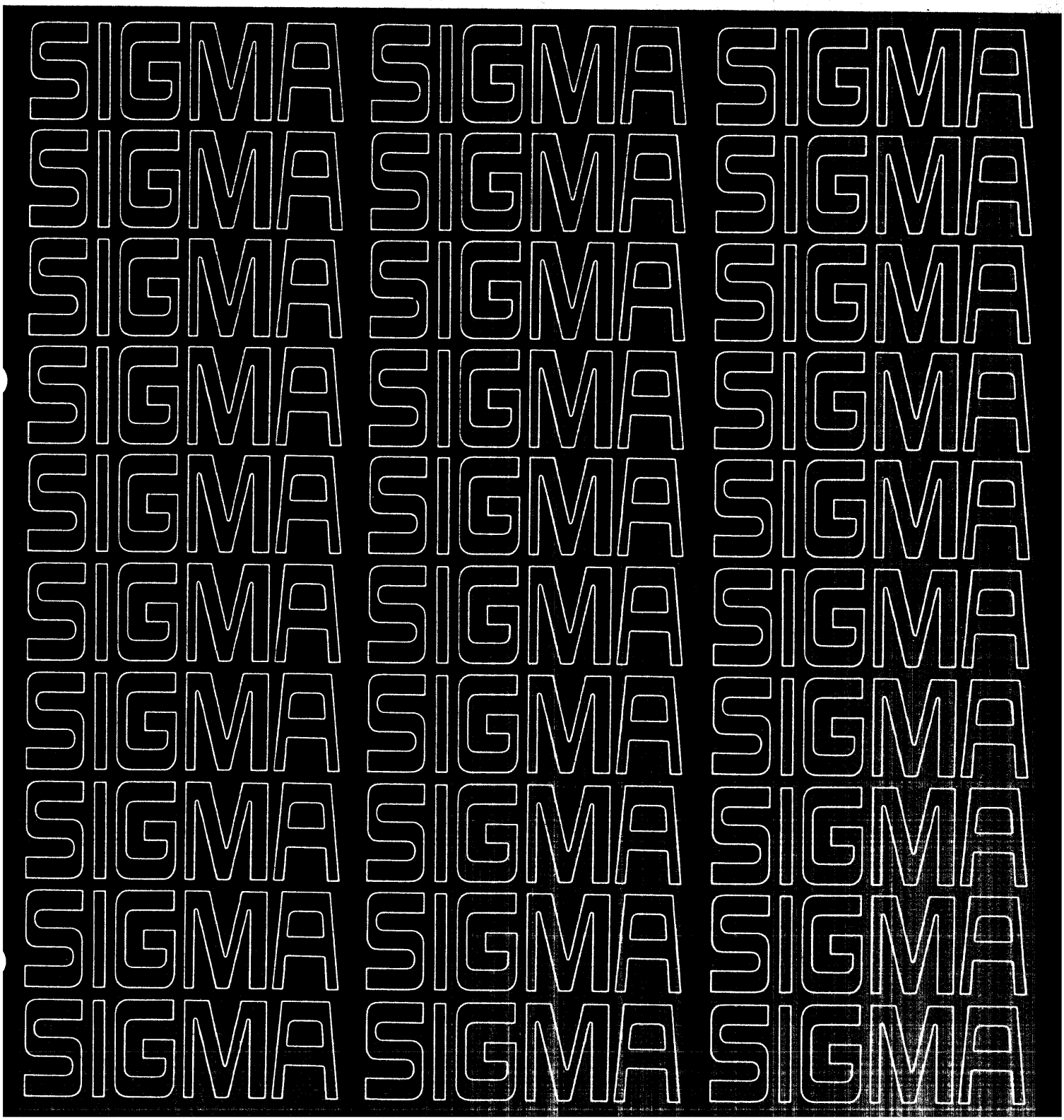
SDS SIGMA SYSTEM INTERFACE UNITS

SCIENTIFIC DATA SYSTEMS



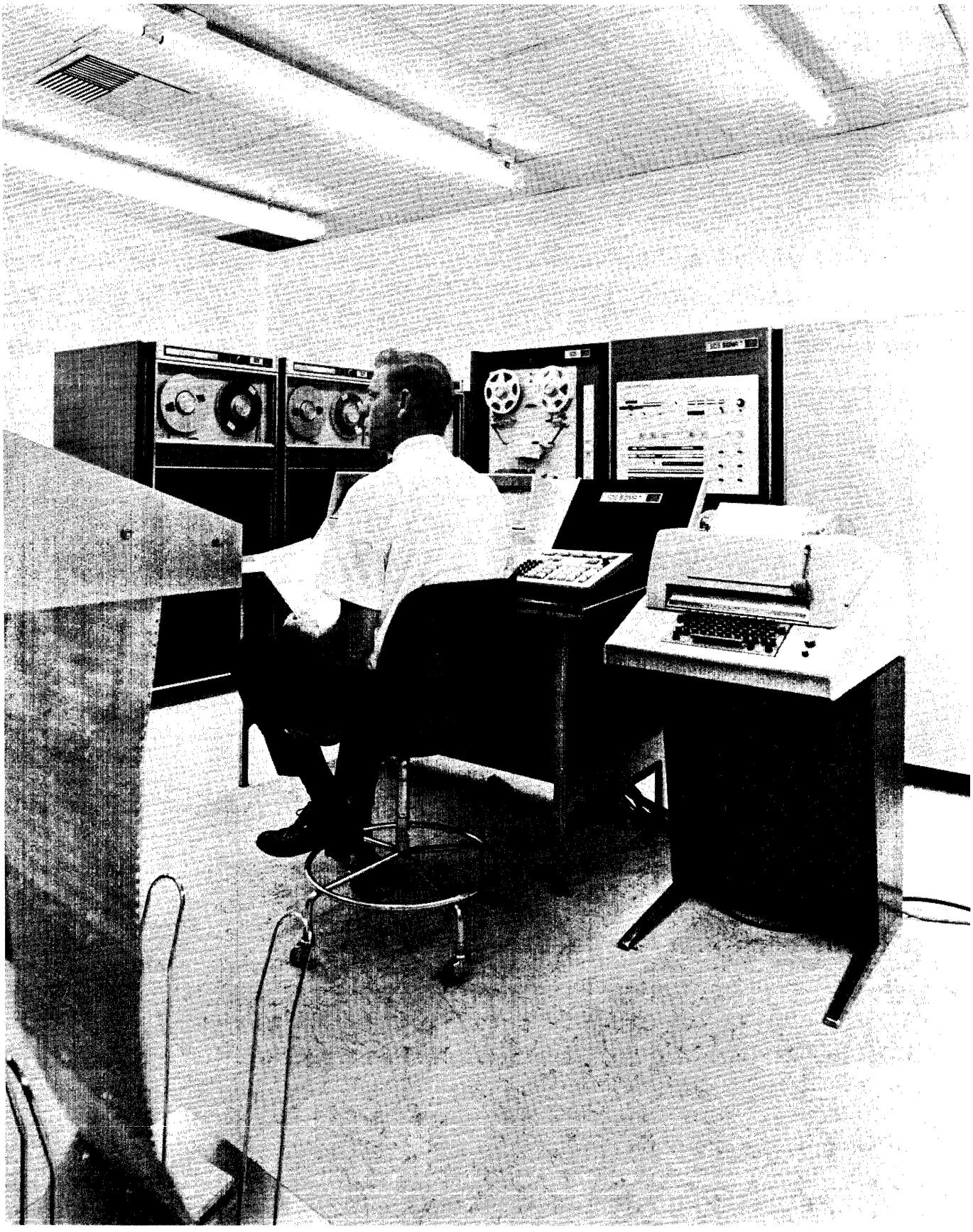
SDS SIGMA SYSTEM INTERFACE UNITS

May 1968

SDS

SCIENTIFIC DATA SYSTEMS • 1649 Seventeenth Street • Santa Monica, California 90404

Standard SDS system interface units link Sigma computer systems, such as the Sigma 7 configuration shown here, to external analog and digital devices.



CONTENTS

PREFACE

Scientific Data Systems bases its total systems capability on a building-block philosophy that the company applies to the design of all its products. This philosophy enables SDS to use standard off-the-shelf products for a wide variety of complex system applications.

Ease of system integration was a primary goal in the design of SDS Sigma computers and their related hardware and software. As a result, an estimated 95 percent of all Sigma 7 systems, for example, can be built up from standard SDS hardware and require no special systems engineering. Standardized system interface units (SIUs), described in this brochure, are a major factor in facilitating Sigma system implementation.

To meet user needs across the entire spectrum of computing, processing, data acquisition, and control applications, SDS provides a comprehensive range of products within the following categories:

- Computers and related main-frame options (memories, interrupts, etc.);
- Peripheral equipment (such as card readers and punches, magnetic-tape units, disc files, line printers, and keyboard displays);
- System interface units;
- Digital field recording systems for seismic applications;
- Logic modules; and
- Analog instruments.

SDS also offers extensive capability in the custom-designing of equipment to meet individual customer requirements, including special programming support as required.

The SDS Computer Systems Division effectively complements SDS computer capabilities by providing, within the over-all SDS organization, an integrated engineering and manufacturing operation that is totally devoted to systems work. By applying the SDS building-block philosophy, this group has produced over 600 special-purpose, custom-designed digital systems to perform a variety of tasks related to telemetry, data acquisition and processing, test facility instrumentation, and seismic exploration.

For information and literature on all SDS products, see your nearest SDS representative. SDS office addresses are listed on the back cover of this brochure.

INTRODUCTION

The design of special systems usually requires that a wide variety of analog and digital devices be connected to the computer itself. To meet this need, SDS manufactures an extensive array of standard system interface units (SUIs). These units permit the computer to serve as the central processing element in special systems such as those used in process control, data acquisition, and data reduction applications.

SDS system interface units exploit the many advanced input/output features of all Sigma computers. The user benefits several important ways including:

- Ease and Speed of System Design. In the past, connecting to a computer's input/output (I/O) interface has presented a considerable problem for the user designing a computer-controlled system. SDS system interface units ease the system designer's task by permitting him to deal with standardized interfaces closely related to his end task. The availability of these units as standard, off-the-shelf products means that system implementation time is sharply reduced; and productive results are achieved sooner.
- User-Oriented Software. Because the SDS system interface units are standard, they are supplied with standard programs, which control and monitor these units in the same manner as they control and monitor standard computer peripheral devices. These programs can operate under the control of standard SDS operating systems (Monitors) for ease of use, especially in real-time applications where foreground/background processing capabilities are required. Time and costs involved in actual use of the equipment are minimized; programming training requirements are reduced.
- Comprehensive Documentation. Thorough and accurate documentation is available for customer inspection and use, even before the hardware is actually delivered. Documentation provided with each of the units described in this brochure includes:

  1. Assembly drawings and module location charts.
  2. Logic equations.
  3. Theory of operation manuals, which help the system logic designer to implement his functional requirements quickly and economically. These manuals include such information as connector locations (and pin numbers) at which various signals are found, the definition of those signals, available unit loads from each signal (or unit loads required), detailed timing diagrams, and logic equations for each unit.

  Also available is the Sigma Computer Systems/Interface Design Manual (SDS Publication No. 900973), which describes logical and electrical characteristics, characteristics of circuits used, various connector pin assignments, and system considerations and includes helpful comments on logic design of units to connect directly to Sigma computers.
- Concurrent Foreground/Background Processing. SDS system interface units are specifically designed to release the computer from the many routine details involved in real-time I/O coupling through direct input/output. Thus, almost all of the system's capacity is available for useful processing. Concurrent processing of a real-time task in the foreground and a general-purpose task in the background is economically sound.
- Present and Future Flexibility. The design of SDS system interface units reflects the thorough research that preceded them, especially in their interaction with other elements in large systems. The resulting flexibility of use assures that current system needs can be met easily and that future system changes and expansions can be made at minimum cost to the user and with minimum disturbance to the existing system.
- Maintenance Programs. A full range of diagnostic and check-out programs is available to facilitate maintenance, thus permitting a high level of off-line check-out or maintenance without hampering normal real-time system operation.
- Lower Costs. Because SDS standard interface units are in full production now, user costs to perform total system functions are appreciably lower.

SIGMA INPUT/OUTPUT STRUCTURE

The architecture of Sigma computers provides three interfaces of different complexity for connection of external equipment. These interfaces offer a range of speed capabilities for input/output data transfers. Manual 900973 provides a more complete discussion of these interfaces.

Direct Input/Output Interface

This interface provides a maximum data transfer rate (including required program control loops) of about 100,000 32-bit words per second. It requires the programmer to exercise more direct control than for alternate interfaces: each input or output data transfer requires the execution of one instruction. However, the cost of the interface and of external units connected to it is minimal.

8-Bit Input/Output Interface

The unique architecture of SDS Sigma computers offers several important advantages including the availability of low-cost data channels. Thus, simultaneous operation of many different equipments is now economically feasible in terms of price/performance tradeoffs. It also means that I/O proceeds independently, and almost all of the central processor's capability is devoted to computation rather than being taken up with servicing input/output on a real-time demand basis.

The 8-bit input/output interface is much higher in performance than the direct I/O interface described previously. It has a maximum data transfer rate to a single device of over 1,125,000 8-bit bytes per second using the selector input/output processor (IOP) of a Sigma 5 or 7 computer. This increases to over 3,000,000 bytes/second when using the 32-bit interface on a selector IOP. A multiplexor IOP permits up to 32 device controllers to be operating simultaneously, with combined maximum data transfer rate exceeding 400,000 bytes per second.

Programming requirements are minimal. After setup, an IOP effectively links each device controller (in turn, as required) directly to memory, thus freeing the Sigma 7 CPU to continue executing a program. Each IOP stores and executes its own program. The computer's program may be stored in some other memory bank to permit maximum throughput rates.

Because of the additional circuitry required to logically time-share a high-bandwidth data and control bus, the cost of connecting external units to this interface is generally higher than the cost of connecting to the direct I/O interface. But the low cost of a data channel now makes simultaneous operation of many different equipments quite feasible in terms of price/performance tradeoffs.

Memory Bus

Direct communication with a Sigma 5 or 7 module through one of the extra ports is made possible by adding one of the multiaccess features (two-way, three-way, or six-way access). I/O rates can thus be as high as the cycle rate of the memory module itself. Because control registers must be built into the external unit, this means of connection to a Sigma system is generally reserved for internal system units (e.g., Multiplexor IOP) but is available to meet special system requirements. This bus is 32 bits wide (plus parity) for Sigma 5 or 7 memories and 16 bits wide (plus parity) for Sigma 2 memories.

SOFTWARE SUPPORT

SDS provides two levels of software support for Sigma series system interface units: (1) Operating System Handlers for both analog and digital input/output and (2) maintenance software including Analog Calibration and Check-Out programs and Digital Check-Out programs. These programs are compatible with software for all standard SDS products.

The major features of the various parts of these programming systems are listed below. See page 27 of this brochure for a more detailed description of standard software.

Operating System Handlers

Operating System Handlers (also called Device Control Routines or Input/Output Handlers) provide the means by which user programs can control the operation of a variety of input/output devices and subsystems.

As part of the general software support for any SDS Sigma system, provision is made for generating a System Monitor at installation time. The System Monitor provides for configuration identification and I/O data handling in a standard modular form. System interface units are identified in the same easy-to-use-and-understand manner as is all other SDS standard peripheral equipment.

Because SDS system interface units are standard, SDS programming systems permit the user to deal with them simply. Even when a real-time program is written in a higher-level language (such as FORTRAN IV), the user can control these units in a variety of convenient ways including the use of subroutines called by the compiler.

Major features of the Operating System Handlers are as follows:

- Standard operating systems (monitors) control handler operation. Critical real-time tasks are processed in the foreground; real-time program checkout and noncritical jobs are processed in the background. Core residency requirements are decreased and ease of use is facilitated because these handlers provide for common services and parameter pools under monitor control.
- Simple CALLs facilitate communication and make the handlers easy to use.
- SIUs are easily controlled by a programmer writing in a higher-level language (such as FORTRAN IV).

- Simple, easy-to-use commands control complex I/O buffering, allowing the user to choose from among a wide variety of operating modes to suit a specific application.

Maintenance and Calibration Software

Analog and digital maintenance and calibration programs are operated under control of the SDS Diagnostic Control Program (DCP). The DCP is designed to permit flexible, dynamic alteration of test parameters in a manner that allows maintenance personnel to diagnose, isolate, repair, and calibrate with minimum down-time.

Here are the major features of the Analog Calibration and Check-Out programs:

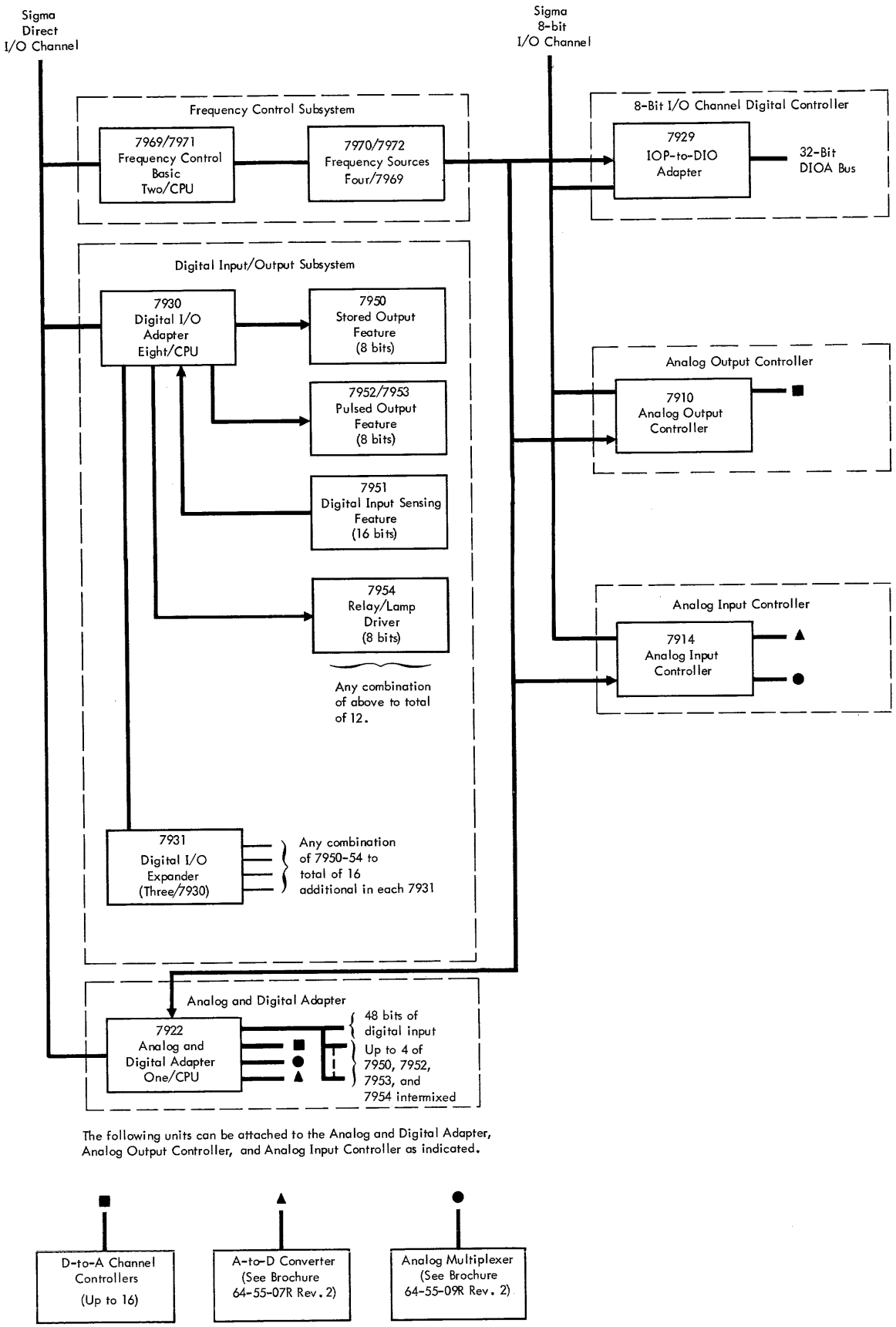
- Time-consuming operator input from the computer console is avoided (for closed-loop testing) since the program automatically searches for channels under test.
- Adjustments on analog multiplexing and conversion equipment are simplified through use of a trace—proportional to full-range inaccuracies of equipment—that a digital-to-analog converter can supply to any lab oscilloscope.
- Operator intervention is minimized since the program automatically compensates for varying equipment scale factors, resolution, and special options.
- Demonstration programs and large-sample programs operate at maximum equipment speeds in a manner designed for worst-case exercising of analog equipment. This feature permits simulating an operating environment for calibration and operation verification
- Hard-copy print-out of accuracy and noise characteristics of the analog devices is provided. Related programs can operate in either an open-loop mode (fixed input and output voltages) or a closed-loop mode (voltages varying across an entire range).

Some of the major features of the Digital Check-Out programs are as follows:

- When equipment configuration permits—that is, when there are at least 8 bits of both input and output—special test cables are provided for use in closed-loop testing of digital input/output. This testing checks all I/O data paths. Test procedures use worst-case patterns that may cause signal interference or may detect marginal circuits.
- Open-loop testing is also provided through use of scope displays.
- Faults are diagnosed down to the lowest possible level for most circuit malfunctions. Print-out indicates probable fault source and other diagnostic information useful in fault location. Thus, system down time caused by equipment malfunction is minimized.
- For demonstration and acceptance purposes, extended-duration tests are available. In such testing, the operator controls test parameter such as data patterns, test duration, and types of tests to be performed.

INTERFACE UNITS AVAILABLE

The available standard SDS interface units for use in Sigma systems are described briefly in Table 1. Installation data is shown in Table 4 on page 31. The configurator on page 4 shows the possible methods of combining these interface control units into a Sigma system. Block diagrams of typical systems that can be constructed through use of these standard units appear on pages 10, 14, and 20.



Sigma System Interface Unit Configurator

Table 1. Sigma System Interface Units

Name of Unit	Model Numbers of Major Elements	Description
Analog Input Controller	7914	Provides the interface and control necessary to operate one A-to-D converter and one high-speed analog multiplexer through a Sigma 8-bit I/O channel. Permits random or sequential sampling of analog inputs at prespecified intervals. Any number of controllers can be added to a Sigma system.
Analog Output Controller	7910	Provides the interface and control necessary to operate one to 16 D-to-A channel controllers through a Sigma 8-bit I/O channel. (Each D-to-A channel controller can operate one to 16 D-to-A converters.) Allows analog outputs to be varied randomly, sequentially, or simultaneously, all at prespecified rates. Any number of controllers can be added to a Sigma system.
Analog and Digital Adapter	7922	Provides the low-cost interface and control circuitry necessary to operate one A-to-D converter, one analog multiplexer, and one to 16 D-to-A channel controllers. Generates pulsed digital outputs, transfers data in memory to output registers, and stores the states of input lines in memory. One unit can be attached to a Sigma system via the direct I/O interface.
IOP-to-DIO Adapter	7929	Transforms any Sigma 8-bit I/O channel into an interface functionally identical to a Sigma Direct I/O interface. Enables user to perform a program-specified number of 32-bit direct input or output operations, in any combination, via the 8-bit I/O channel. Any number of controllers can be added to a Sigma system.
Digital I/O Subsystem	7930 7931 7950 7951 7952 7953 7954	Generates pulsed digital outputs, transfers data in memory to output registers, stores the states of input signals in memory, and provides latched relay drive signals. Each fully expanded unit accommodates any combination of 8-bit stored output groups, 8-bit relay drive groups, 8-bit pulsed output groups, or 16-bit input groups up to a total of 60 groups. One to eight units can be added to a Sigma system via the direct I/O interface.
Frequency Control Subsystem	7969 7970 7971 7972	Provides means of frequency control for SDS analog input, analog output, and digital transfer control units, thus enabling external devices to perform operations at regular prespecified intervals. Each fully expanded unit furnishes four independent frequency sources. Frequency of each source can be specified either manually or by program. One or two units can be used in a Sigma system.
Device Subcontroller	7900	Provides means for standardizing certain common parts of device controllers that, in turn, connect a customer's device or signals to the 8-bit I/O channel interface on a Sigma computer. The Model 7900 Subcontroller permits quicker design and checkout of custom-designed equipment and improves maintainability. It can duplicate certain common functions that must be present in all equipment attached to the 8-bit Sigma interface. This subcontroller is an integral part of all SDS standard peripheral controllers that connect to the 8-bit Sigma interface.

The SDS Model 7914 Analog Input Controller offers a flexible, economical means of connecting analog-to-digital conversion equipment to SDS Sigma computers. Under control of this unit, analog inputs can be sampled randomly or sequentially at prespecified intervals. Once initiated, analog-to-digital (A-to-D) conversions proceed independently of the Sigma central processor. An interconnection diagram of the Model 7914 appears in Figure 1.

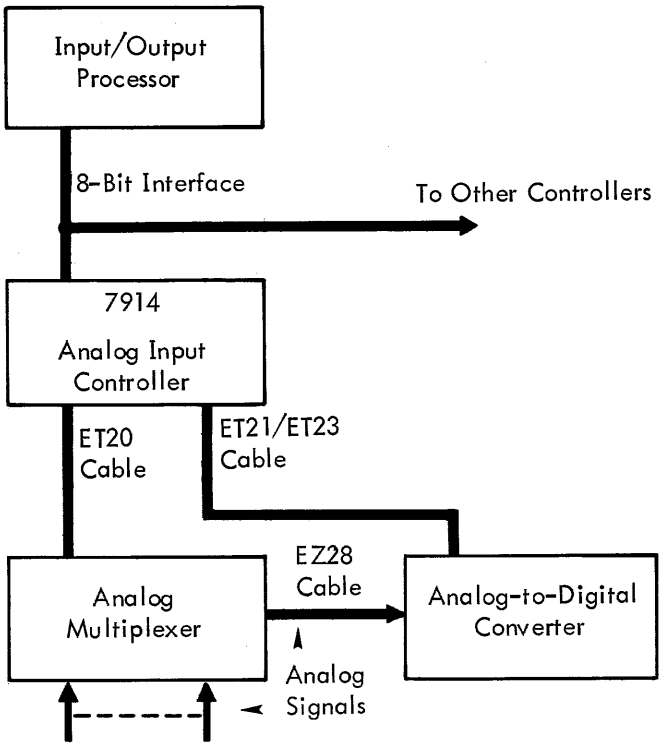


Figure 1. Interconnection Diagram, SDS Model 7914 Analog Input Controller

DESCRIPTION

The Model 7914 controller operates through an 8-bit I/O channel of a Sigma computer. It connects directly to the 8-bit I/O interface where it uses one channel position. Each Model 7914 provides the interface and control necessary to operate one high-speed analog multiplexer and one analog-to-digital converter.

The Model 7914 was designed primarily for use with SDS A-to-D conversion equipment and SDS analog multiplexers. However, its interface also allows other manufacturers' analog conversion equipment to be connected to a Sigma computer.

SDS A-to-D conversion equipment and SDS analog multiplexers are described in brochure 64-55-07R (Rev. 2) and 64-55-09R (Rev. 2), respectively.

OPERATION

Two program-selectable modes of operation are possible with the Model 7914: (1) the random mode, in which the computer supplies a new multiplexer address before each conversion, and (2) the sequential mode, in which the computer supplies a multiplexer channel address for the first conversion only. (The multiplexer then generates subquent addresses.)

When operating in Mode 2, channel addresses for subsequent conversions are generated in one of the following two ways:

1. By incrementing the present address by one before each conversion.*

2. By maintaining the same address for all conversion in a group. In this case, the 7914 need not wait for the multiplexer to settle before initiating each conversion since the channel address has not changed.

After activation by an SIO instruction, the 7914 requests the first order. In response, the I/O channel accesses the first order from main memory, transmits that order to the 7914, and stores internally all remaining command information. The order transmitted to the 7914 is "Read" (binary configuration 00000010).

Command information stored internally by the I/O channel includes (1) the memory address of the first byte to be output, (2) a count of the number of bytes to be transferred, (3) a set of flags that control the I/O channel's response upon detection of certain conditions, and (4) such other control information as the I/O system requires.

After the 7914 receives the Read order, it accesses the first two bytes of a program-specified list in memory. These bytes specify a multiplexer channel address and certain control information describing the mode of operation. When the subsequent multiplex-conversion cycle has been completed, the digital result from the A-to-D conversion is stored in memory in the two byte locations following those just accessed for control and multiplexer address.

*If the A-to-D converter has a sample-and-hold feature, the multiplexer channel address can be incremented as soon as the previous conversion has been initiated, thereby increasing sampling rate. This is known as an "overlap" mode of operation.

In the random mode of operation, the 7914 accesses the next two bytes in sequence containing the new multiplexer address and control information, thereby initiating a new multiplex-conversion cycle. This process (i.e., 7914 access of address and control information and storage of digital result of A-to-D conversion) repeats until the program-specified number of analog samples has been obtained.

In the sequential mode of operation, the first two bytes obtained by the 7914 have the same format as those in the random mode (i.e., multiplexer address and control information). Thereafter, converted digital data is packed into successively higher byte pairs until the program-specified number of analog samples has been obtained. The control information contained in the first byte accessed by the 7914 determined whether the multiplexer address for each successive conversion is either incremented by one or remains the same.

Each multiplex-conversion cycle is initiated either immediately upon completion of the previous cycle (maximum rate permitted by equipment) or only after an external signal occurs. This signal can be supplied by the SDS Model 7969 Frequency Control Unit. When operated in this manner, the 7914 allows the user to sample analog inputs at regular prespecified intervals.

The multiplexer and A-to-D conversion equipment and interaction with the 7914 determine the maximum sampling rate of the analog signals.

Sampling times for four typical configurations using SDS A-to-D conversion equipment with SDS MU55 multiplexers are listed in the following tabulation (these operating rates assume no conflict with other devices on the 8-bit I/O bus):

SDS A-to-D Converter	Operation Mode of 7914	Time per Sample (μsec)	Sampling Rate
AD30-12*	Random	70.0	14.1 kc
AD30-12†	Sequential (step)	35.0	28.5 kc
AD35*	Random	41.5	24.1 kc
AD35-SH†	Sequential (step)	23.2	43.9 kc

*Without sample-and-hold
†With sample-and-hold

The 7914 indicates an "unusual end" condition to the I/O channel and terminates operation if it detects either of the following conditions:

- I/O channel halt (IOP halt); or
- Incorrect byte string length.

PROGRAMMING

The Model 7914 Analog Input Controller is programmed using standard Sigma input/output instructions (SIO, TIO, HIO, TDV, and AIO). Eight toggle switches on the 7914 determine the device address to be used in I/O instructions when communicating with this unit.

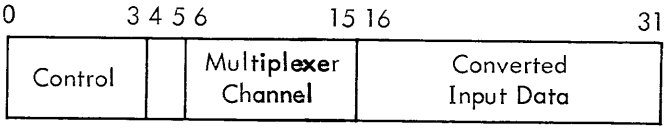
Status response returned during execution of SIO, TIO, and HIO is as follows:

- Interrupt pending from 7914
- 7914 is either ready or busy
- The last operation (multiplexer-conversion cycle) was terminated because of unusual conditions
- The 7914 recognized the program-specified device address
- The 7914 can accept an SIO (returned during TIO only)
- SIO instruction was executed successfully (returned during SIO only)
- The 7914 was busy when the HIO instruction was executed (returned during HIO only)

By means of the TDV instruction, the program can determine (1) whether a multiplexer is connected, (2) whether a sample-and-hold is connected, and (3) whether a frequency control unit is connected. Thus, programming need not be system-dependent.

Status returned during the execution of the AIO instruction determines the reason for interrupt.

The word format for all words of the program-specified list in the random mode and for the first word in the sequential mode is as follows:



Bit Positions 0 through 3, Control

Bit 0

A "zero" causes unit to operate in random mode
A "one" causes unit to operate in sequential mode

Bit 1

A "zero" causes unit to operate at a maximum rate permitted by the equipment (multiplexer/A-to-D converter interaction)

A "one" causes unit to operate under control of an external signal to initiate conversion

Bit 2 (used only in sequential mode)

A "zero" causes the multiplexer address to be incremented by one for each conversion

A "one" causes the multiplexer address to remain unchanged for each conversion

Bit 3 (must be zero unless bit 1 is set)

A "zero" causes no action

A "one" causes the unit to operate in a burst mode in which all samples in a program-specified block are taken as quickly as possible. However, operation does not begin until an external signal occurs.

Bits 4, 5

Unused

Bits 6-15, Multiplexer Channel Address

These bits specify multiplexer channel address to be used for the next conversion; alternatively, users' equipment can elect to treat three or four of these bits as gain control information.

Bits 16-31, Converted Input Data

These bits contain left-adjusted converted digital data from the A-to-D converter.

INTERFACE

Two connectors are provided for the operation of analog conversion and multiplexing equipment. One of these is used for connecting an analog multiplexer. The other is used to operate an A-to-D converter.

The multiplexer connector carries the following signals:

Multiplexer Load — a pulse of 1.0-μsec duration. This pulse indicates that a multiplexer channel address is presently available on the multiplexer data lines.

Multiplexer Data Lines 0-7 — eight lines that carry the multiplexer channel address for a period beginning with the leading edge of the load pulse and ending 0.5 μsec after the trailing edge of that pulse.

Multiplexer Step — a pulse of 1.0-μsec nominal duration, which causes the multiplexer channel address to be incremented by one.

Multiplexer Ready — a pulse of 1.0-μsec minimum duration that must be supplied by the multiplexer to indicate the end of its settling interval.

The A-to-D converter connector provides the following signals:

Convert — a pulse of 1.0-μsec nominal duration that causes the A-to-D converter to initiate a conversion cycle.

End of Convert — a pulse of 0.3- to 1.0-μsec duration that must be supplied by the A-to-D converter to indicate its completion of a conversion cycle.

Strobe—a pulse of 1.0 μsec duration that indicates to the A-to-D converter that its digital output is being read by the 7914.

Data Lines — 16 data lines that carry the digital output from the A-to-D converter to the 7914. These lines must be stable during the interval ranging from 0.5 μsec before the trailing edge of the strobe pulse to 0.3 μsec after the trailing edge of the strobe pulse.

External equipment mates to the connectors on the 7914 by means of an SDS ZT15 Cable Plug Module. Standard connection to SDS analog instruments is made via ET20, ET21, or ET23 cables.

All signals are quiescent at +8 volts (high impedance) and active at 0 volts, thereby permitting transformer coupling of all signals in the analog instruments.

For a more complete discussion of Sigma I/O programming, see applicable Sigma Reference Manuals.

The SDS Model 7910 Analog Output Controller provides a flexible and economical method for connecting digital-to-analog conversion equipment to an SDS Sigma computer. Analog outputs can be made to vary randomly, sequentially, or simultaneously within a program-specified group at a predetermined rate, under control of the Model 7910. Once initiated, conversions proceed independently of the CPU.

DESCRIPTION

The Model 7910 Analog Output Controller operates through an 8-bit I/O channel of a Sigma system. It connects directly to the 8-bit interface and utilizes one 8-bit channel.

The 7910 can connect to and control up to 16 digital-to-analog channel controllers. SDS offers three models of channel controllers, with a variety of D-to-A converters available for each of them. These three models, all of which can be controlled by a 7910, are:

- DA35-9 — Controls one to sixteen 9-bit D-to-A converters (Model DX15).
- DA35-15 — Controls one to five 12-bit or 15-bit D-to-A converters in any combination (Models DX16, DX17, DX26, or DX27).
- DA36-15 — Controls one to twelve 12-bit or 15-bit D-to-A converters in any combination (Models DX16, DX17, DX26, or DX27).

OPERATION

SDS D-to-A converters are implemented with dual-rank holding registers in which contents of the second-rank register are continuously converted to an analog signal. Altering contents of the first-rank register does not affect contents of the second-rank register and, consequently, does not affect the analog output.

A specific signal must be issued to the D-to-A converter to cause the contents of its first-rank register to transfer to the second-rank register, thereby producing a new analog output after a short settling interval. This transfer signal, generally referred to as a "convert" command, is supplied simultaneously to all D-to-A converters connected to a particular 7910 Analog Output Subsystem. Only the analog output of the D-to-A converters whose first-rank register has been altered since the previous transfer signal occurred will change.

An interconnection diagram for the Model 7910 Analog Output Controller is shown in Figure 2.

To fully use the dual-rank feature, the analog output controller operates in either of two program-selectable modes:

Mode 1 — Contents of the first-rank register transfer to the second-rank register as soon as the first-rank register of the currently selected D-to-A converter has been loaded. This transfer causes a new analog output to appear on a channel shortly after digital data is received from the 8-bit interface.

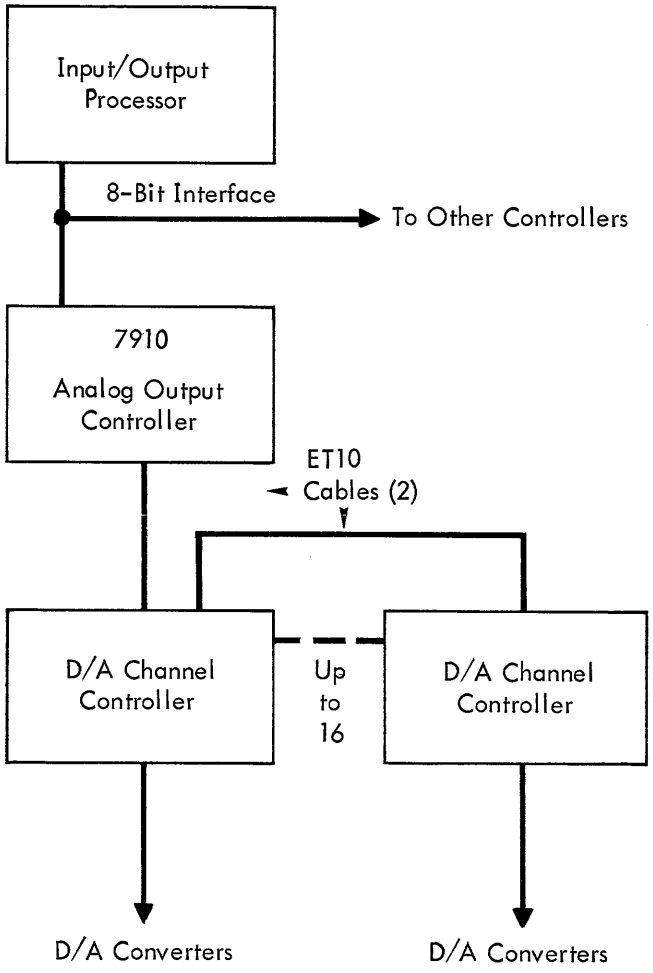


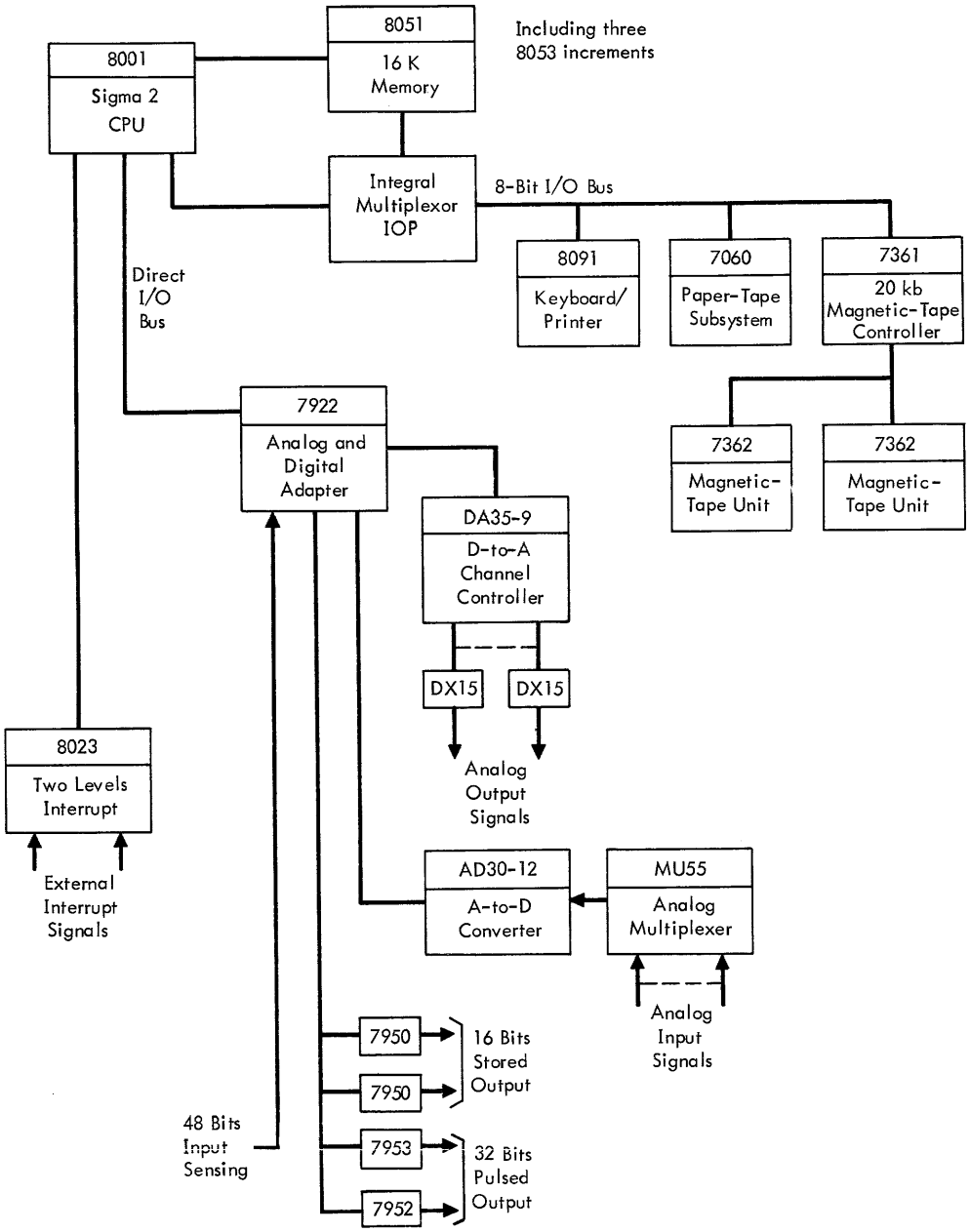
Figure 2. Interconnection Diagram, SDS Model 7910 Analog Output Controller

Mode 2 — Transfer to the second-rank register occurs only after an entire group of first-rank registers has been loaded. This transfer causes new analog outputs to appear simultaneously from all second-rank registers in the group.

The actual transfer pulse can be generated either by the 7910 or by an external source, which supplies it to the 7910. In the latter case, the SDS frequency control subsystem, described on page 24, can be used to provide the external transfer pulse. Operating in this way, specific groups of analog outputs can be caused to change randomly, sequentially, or simultaneously at regular prespecified intervals. An SIO instruction initiates operation of the 7910, which then requests the first order from the I/O system. In response, the I/O system transmits the "Write" order (binary configuration 00000001) to the 7910 and stores all remaining command information internally.

Command information stored internally by the I/O system includes (1) the memory address of the first byte to be output; (2) a count of the number of bytes to be transferred; (3) a set of flags, which control the I/O system response upon detection of certain conditions; and (4) such other control information as the I/O system requires.

After the 7910 receives the Write order, it begins accessing information four bytes at a time from a program-specified list in computer memory. Four bytes of information are required for each conversion — one control byte, one D-to-A converter address byte, and two



Typical Small Analog/Digital Acquisition and Control System

digital data bytes. Transfer/conversion cycles continue independently of the CPU until the program-specified number of conversions has been made.

The 7910 indicates "unusual end" to the I/O system and stops operating if it detects either of the following conditions:

- I/O channel halt (IOP halt) or
- Frequency control unit causes a rate error.

The 7910 indicates "channel end" to the I/O system when it has initiated conversion of the last digital output in the list.

D-to-A converter updating rate is approximately 80 kc if no other devices are operating on the 8-bit I/O bus.

PROGRAMMING

Standard Sigma I/O instructions (SIO, TIO, HIO, TDV, AIO) are used in programming the 7910 Analog Output Controller. Eight toggle switches on the 7910 determine the device address that must be used by the I/O instructions when communicating with that unit.

Status response returned during execution of SIO, TIO, and HIO is as follows:

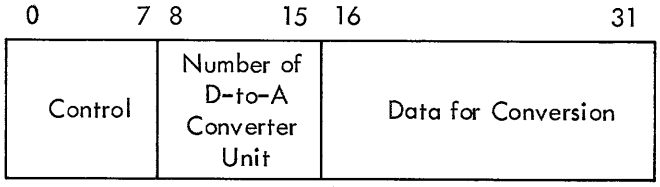
- Interrupt pending from 7910;
- 7910 is either ready or busy;
- The last output operation was terminated because of unusual conditions;
- The program-specified device address was recognized by the 7910;
- SIO can be accepted (TIO only);
- SIO was successful (SIO only); and
- The 7910 was busy when HIO was executed (HIO only).

Status response returned during execution of TDV is as follows:

- Rate error occurred on last operation, and
- Whether frequency control unit is connected.

Status, returned during the execution of the AIO instruction, provides the reason for interrupt.

The four bytes received by the 7910 during each conversion cycle have the following format:



Bits 0 through 7 control the action taken by the addressed D-to-A converter upon receipt of the data for conversion as follows:

Bits Positions 0 and 1

00 Load first-rank register of addressed D-to-A converter but perform no other action.

01 Load first-rank register of addressed D-to-A converter, and then transfer first-rank register to second-rank register in all D-to-A converters connected to the 7910, thus altering their analog output.

NOTE: If the first-rank register of a particular D-to-A converter has not been changed since the last transfer, there will be no change in its analog output.

11 Load first-rank holding register of the addressed D-to-A converter, but inhibit all further operations of the 7910 until the occurrence of an external transfer signal. The occurrence of this signal causes transfer from the first-rank register to the second-rank register in all D-to-A converters connected to the 7910 and resumption of 7910 communications with the I/O system.

Bit Positions 2 through 7

Unused

Bit Positions 8 through 11

Specify one of 16 possible D-to-A channel controllers.

Bit Positions 12 through 15

Specify one D-to-A converter connected to the addressed D-to-A channel controller.

Bit Positions 16 through 31

Contain the digital data word to be converted, which must be left-justified with the most significant bit being the sign bit (two's complement).

INTERFACE

The 7910 provides for connecting 16 D-to-A channel controllers. Two 14-conductor cables constitute a data/control bus from which each channel controller receives necessary information.

Signals appearing on each connector are:

Data Line 0 through Data Line 15

16 lines, containing data for conversion, that remain stable during the time the Channel Select strobe occurs.

Channel Select Lines 0 through 7

Eight lines that indicate the D-to-A converters on the selected D-to-A channel controller to be activated. Decoding is performed by the D-to-A channel controllers. These lines are stable during the time the Channel Select strobe occurs.

Channel Select Strobe

A strobe signal indicating when the channel select lines are valid. Pulse duration is 1.0 μsec nominal.

Convert Line

Common for all D-to-A channel controllers (nominal duration of 1.0 μsec). This line, when true, enables transfer from the first-rank to the second-rank register in all attached D-to-A converters. Using the control byte previously described, the program determines the activation time.

AT12 cable driver modules are used for all signals. All cabling to the SDS D-to-A converters is by means of two ET10 cables. Transformer coupling is not available when using the 7910.

The SDS Model 7922 Analog and Digital Adapter is a control device for use with a wide range of instruments that interface Sigma computers to analog devices. Use of the versatile Model 7922 in any Sigma system is indicated when the need for economy overrides the need for high performance. It consists of one SDS T-Series card cage with the basic modules inserted and wired. The same cage contains modules for the control options.

DESCRIPTION

The basic Model 7922 can control one SDS Model AD30-12, AD30-15, AD-35, or AD35-SH Analog-to-Digital (A-to-D) converter. Available for use with these converters, as needed for high-level requirements, is the SDS MU Series of solid-state analog multiplexers, which can also be controlled by the 7922.

The 7922 can control one to 16 D-to-A channel controllers. SDS manufactures three D-to-A channel controllers:

- DA35-9 Accommodates up to 16 D-to-A converters with 9-bit resolution (Model DX15)
- DA35-15 Accommodates up to five D-to-A converters with 12-bit resolution (Model DX16 or DX26) or 15-bit resolution (Model DX17 or DX27)
- DA36-15 Accommodates up to 12 D-to-A converters with 12-bit resolution (Model DX16 or DX26) or 15-bit resolution (Model DX17 or DX27)

The Model 7922 can perform various types and quantities of digital input/output when it is used with the following units:

- Model 7950 Stored Digital Output (8 bits);
- Model 7952 (quiescent +4 volts) or Model 7953 (quiescent 0 volts) Pulsed Digital Output (8 bits); and
- Model 7954 Relay Driver (8 bits).

The only limitation here is that the total number of 7950s plus 7952s plus 7953s plus 7954s cannot exceed four.

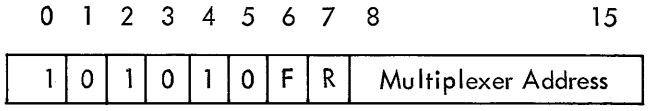
As part of its basic capability, the 7922 can sense the state of 48 input signal lines. Figure 3 is an interconnection diagram of the Model 7922 unit, only one of which may be used in each Sigma system.

OPERATION AND CONTROL

All control and data transfer operations that the 7922 can perform are executed by Read Direct (RD) and Write Direct (WD) instructions in any Sigma computer. Hence, an external interface feature is a prerequisite.

Analog Input Control

A single RD instruction controls the A-to-D converter and the analog multiplexer. Word format of the effective address of the RD instruction is interpreted as follows:



Executing this instruction initiates the following action:

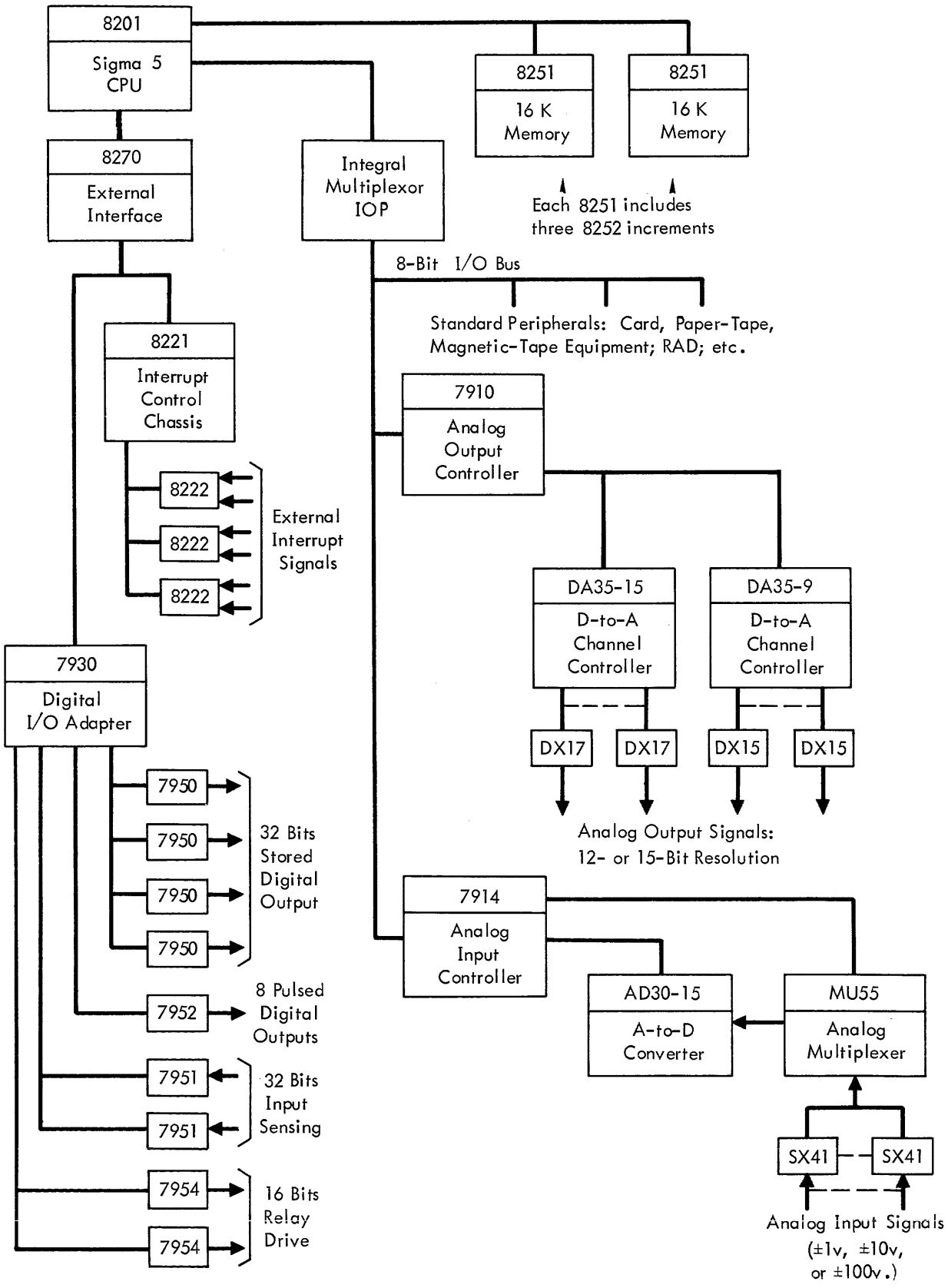
1. If the previous A-to-D conversion is complete (or if this is the first such instruction executed since power-on), the digital results of that conversion are returned to the low-order 16-bit positions of the designated register* (left-adjusted within that area unused bits are returned true), and status line 1 is returned "false." This resets condition code 3 in Sigma 7†.

If R (bit 7) is a "zero," the multiplexer channel address specified in bits 8 through 15 is loaded in the multiplexer's channel address register. At the conclusion of the multiplexer's settling interval, a new conversion is automatically initiated on the A-to-D converter if F (bit 6) is a "zero." If F is a "one," the ADC conversion is delayed until an external signal (e.g., the output of a 7969 frequency control subsystem) is received.

If R is a "one," the multiplexer address (bits 8 through 15) is ignored, and a conversion is automatically initiated upon the previously selected channel (thus eliminating the multiplexer's settling interval) if F is a "zero." If F is a "one," conversion is delayed until an external signal is received. The SDS Model 7969 Frequency Control Unit can supply this signal.

2. If the previous A-to-D conversion is not complete at the time this instruction is executed, or if the controller is waiting for an external signal, condition code 3 is set†; and no other operations are allowed to take place.

*The accumulator in Sigma 2.
†Overflow indicator in Sigma 2.



Typical Medium Analog/Digital Subsystem

3. The 7922 generates a signal upon completion of the A-to-D conversion, and this signal can be coupled to any external priority interrupt installed in the system.

Analog Output Control

A single WD instruction controls the D-to-A converters attached to the 7922. Word format for the effective address of the WD instruction is interpreted as follows:

0	1	2	3	4	5	6	7	8 ... 15
1	0	1	0	1	0	F	C	D-to-A Converter Channel Select

Execution of this instruction initiates the following action:

1. The first-rank register of the D-to-A converter, specified by bits 8 through 15 of the effective address, is loaded with the 9, 12, or 15 most significant bits of the low-order 16 bits of the designated register (or the accumulator in Sigma 2).

2. If C (bit 7) is a "zero," no further action is taken.

3. If C is a "one" and F (bit 6) is a "zero," the first-rank registers of all D-to-A converters in the system are loaded into their respective second-rank registers, thus causing a "new conversion" on all converters whose first-rank registers were altered since the previous "convert" command.

4. If C is a "one" and F is a "one," the loading of the second-rank DAC registers is delayed until an external signal is received. The SDS Model 7969 Frequency Control Unit can supply this signal.

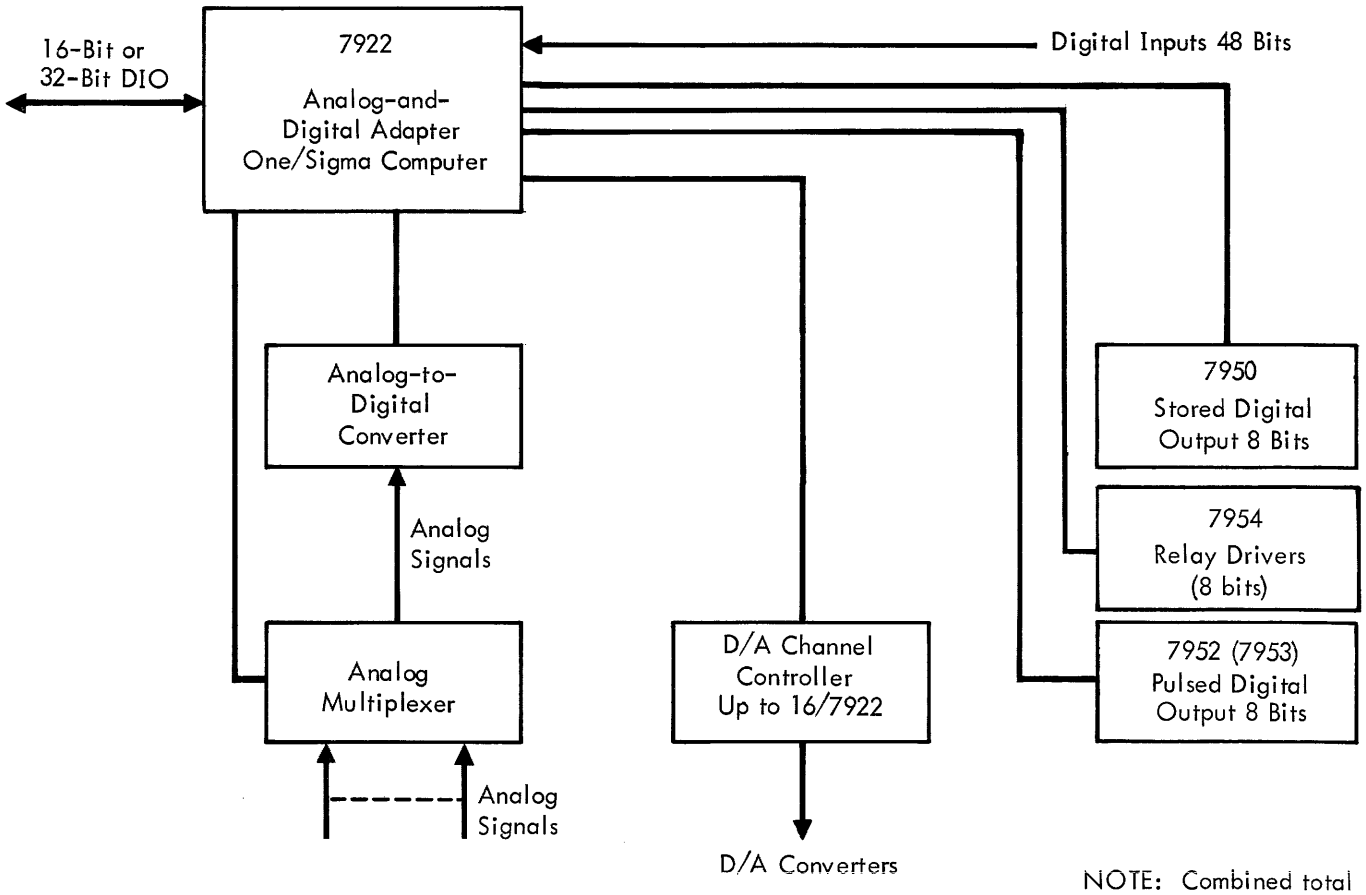


Figure 3. Interconnection Diagram, SDS Model 7922 Analog and Digital Adapter

5. The 7922 generates a signal upon initiation of conversion, and this signal can be coupled to any external priority interrupt installed in the system.

6. If the D-to-A conversion has been requested previously but has not been completed at the time this instruction is executed, condition code 3 is reset; and no other operations are allowed to take place.

The D-to-A converter channel selection codings in bits 8 through 15 of the effective address are as follows:

- Bits 8 to 11 select one of the 16 possible channel controllers.
- Bits 12 through 15 select one of the 16 possible converters in the designated channel controller.

Control of Digital I/O Transfers

The RD and WD instructions, respectively, control all digital input and output transfers possible with the 7922.

RD instructions permit storage of a specified set of 16 input lines (out of 48) in the designated register (Sigma 5 and Sigma 7) or the accumulator (Sigma 2). The following address configuration must be used:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	0	1	1	0	0	0	0	0	0	0	R_1	R_2	R_3

R_1, R_2, and R_3 select one of the three 16-bit words to be read into the computer.

WD instructions permit control of output groups, either 8 bits or 16 bits at a time. The following address configuration must be used:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	0	1	1	0	0	0	0	D_1	D_2	B_0	B_1	B_2	B_3

D_1 and D_2 specify the duration of the output pulse generated when 7952/53 modules are installed. The bit configuration and output pulse duration are as follows:

D_1	D_2	Output Pulse Duration
0	0	1 μsec
0	1	2 μsec
1	0	3 μsec
1	1	4 μsec

B_0, B_1, B_2, and B_3 select bytes (I/O modules) to be output. Since the 7922 only utilizes 16 bits of the data bus regardless of Sigma computer type (2, 5, or 7), 1100 or 0011 must be used for maximum control.

When a digital output transfer (WD) is being executed, condition code 4 will be returned "false" if the external device is ready; however, the data transfer can still be completed. When a digital input transfer (RD) is being executed, condition code 4 is returned "true" if the external device is ready.

INTERFACE

Two connectors are provided for the operation of analog-to-digital conversion and multiplexing equipment. One of these is used for connecting an analog multiplexer. The other is used to operate an A-to-D converter.

The multiplexer connector carries the following signals:

Multiplexer Load—a pulse of 1.0-μsec duration. This pulse indicates that a multiplexer channel address is presently available on the multiplexer data lines.

Multiplexer Data Lines 0-7—eight lines that carry the multiplexer channel address for a period beginning with the leading edge of the load pulse and ending 0.5 μsec after the trailing edge of that pulse.

Multiplexer Ready—a pulse of 1.0-μsec minimum duration that must be supplied by the multiplexer to indicate the end of its settling interval.

The A-to-D converter connector provides the following signals:

Convert—a pulse of 1.0-μsec nominal duration that causes the A-to-D converter to initiate a conversion cycle.

End of Convert—a pulse of 0.3- to 1.0-μsec duration that must be supplied by the A-to-D converter to indicate its completion of a conversion cycle.

Strobe—a pulse of approximately 4.0-μsec duration that indicates to the A-to-D converter that its digital output is being read by the 7922.

Data Lines—16 data lines that carry the digital output from the A-to-D converter to the 7922. These lines must be stable during the interval ranging from 0.5 μsec before the trailing edge of the strobe pulse to 0.3 μsec after the trailing edge of the strobe pulse.

External equipment mates to the connectors on the 7922 be means of an SDS ZT15 Cable Plug Module. Standard connection to SDS analog instruments is made via ET20, ET21, or ET23 cables.

All signals are quiescent at +8 volts (high impedance) and active at 0 volts, thereby permitting transformer coupling of all signals in the analog instruments.

The 7922 provides for connecting 16 D-to-A channel controllers. Two 14-conductor cables constitute a data/control bus from which each channel controller receives necessary information.

Signals appearing on each connector are:

Data Line 0 through Data Line 15

> 16 lines, containing data for conversion, that remain stable during the time the Channel Select strobe occurs.

Channel Select Lines 0 through 7

> Eight lines that indicate the D-to-A converters on the selected D-to-A channel controller to be activated. Decoding is performed by the D-to-A channel controllers. These lines are stable during the time the Channel Select strobe occurs.

Channel Select Strobe

> A strobe signal indicating when the channel select lines are valid. Pulse duration is 1.0-μsec nominal.

Convert Line

> Common for all D-to-A channel controllers (nominal duration of 1.0 μsec). This line, when true, enables transfer from the first-rank to the second-rank register in all attached D-to-A converters. Using the control byte previously described, the program determines the activation time.

AT12 cable driver modules are used for all signals. All cabling to the SDS D-to-A converters is by means of two ET10 cables. Transformer coupling is not available when using a 7922.

The SDS Model 7929 IOP-to-DIO Adapter permits a standardized interface for external devices to be used in a Sigma computer system. The unit makes the standard Sigma system 8-bit interface (IOP) identical to the Sigma direct input/output interface (DIO). Thus any unit designed for use on the Sigma DIO interface (e.g., 7922, 7930) can be operated instead in a cycle-stealing mode by connecting it to the 7929's DIO Alternate (DIOA) interface.

With the Model 7929, the user can perform a program-specified number of Read Direct (RD) or Write Direct (WD) operations in any combination without CPU intervention after the operation is initiated.

The TDV instruction enables the program to determine (1) whether a rate error has occurred, (2) the status response currently stored within the 7929, (e.g., CC3 and CC4), and (3) certain other diagnostic information.

DESCRIPTION

The Model 7929 operates through an 8-bit I/O channel of a Sigma system. It connects directly to the 8-bit interface where it uses one 8-bit channel. Each 7929 added to an I/O channel provides a completely independent direct input/output interface.

Figure 4 is an interconnection diagram of the Model 7929.

OPERATION

Upon activation by an SIO instruction, the 7929 requests the first order from the I/O channel. In response, the Sigma I/O system transmits the order (8 bits) to the 7929 and internally stores all remaining command and control information. The order transmitted to the 7929 is ignored by the 7929 nor will it generate an interrupt.

Command information stored internally by the I/O channel includes: (1) the memory location of the first byte to be transferred, (2) a count of the number of bytes to be transferred, (3) a set of flags that control the I/O channel's response upon detection of certain conditions, and (4) such other control information as the I/O system requires.

After receiving the Write order, the Model 7929 stores the condition code settings returned during its previous operation in the first byte location of a program-specified list in memory. Then the unit sequentially accesses the next three bytes from the list. These bytes include one control byte and a 16-bit address.

If the control byte specifies a Write Direct operation, the 7929 sequentially accesses the next four bytes from the list. These bytes form a 32-bit data word. The address and data are then transferred simultaneously to the connected external devices. The device specified by the 16-bit address must respond by accepting the 32-bit data word and returning status conditions to the 7929 together with an acknowledge signal.

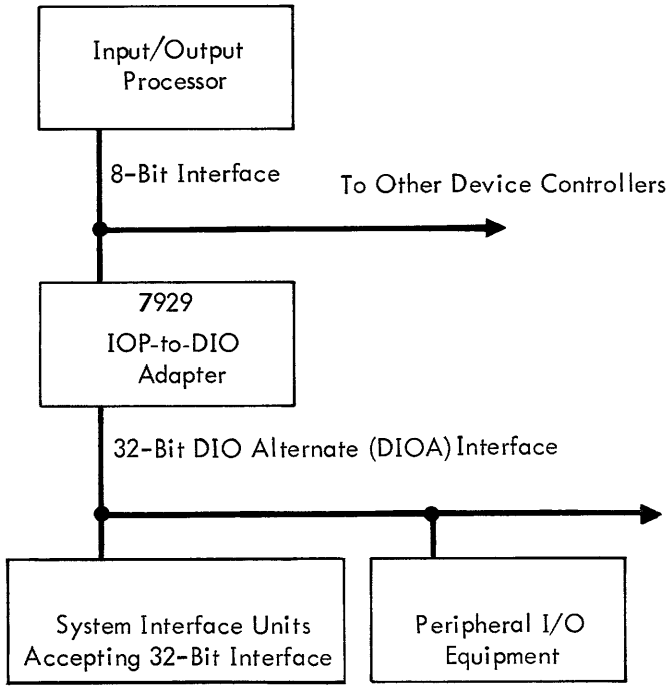


Figure 4. Interconnection Diagram, SDS Model 7929 IOP-to-DIO Adapter

Upon receiving the acknowledge signal, the 7929 stores the status conditions in bits 2 and 3 of the next sequential byte location in the list.

If the control byte specifies a Read Direct operation, the 7929 transmits the 16-bit address to connected external devices. The addressed device must respond by supplying a 32-bit data word and status conditions to the 7929 together with an acknowledge signal.

Upon receiving the acknowledge signal, the 7929 stores the 32-bit data word in the next four byte locations and the status conditions in bits 2 and 3 of the following byte location.

> NOTE: If either the present Write Direct or Read Direct operation is the last operation in the list, the 7929 stores the status conditions internally and, later, stores them in memory in the first byte location of the subsequent operation list.

Two modes of operation are possible, as determined by the first control byte accessed:

> Mode 1—A new control byte and 16-bit address are supplied with each data word transfer.

Mode 2—The first control byte and 16-bit address accessed apply to all remaining data in a list whose length is program-specified. In this mode, only the status conditions returned during the last operation are stored. These conditions are stored in the first byte location of the subsequent operation list.

The Model 7929 executes Read Direct or Write Direct operations at a rate determined by one of two program-selected criteria:

1. The maximum rate permitted by the interaction of the I/O system, the 7929, and external equipment.

2. Each RD or WD operation is delayed until an external signal occurs. Frequency of occurrence of this signal may vary from 0 to 62.5 kc and may be part of an interactive feedback loop.

The SDS Frequency Control Subsystem, described on page 24, can supply the external signal. When operated in this manner, the 7929 can execute Read Direct or Write Direct operations in any combination at a prespecified rate. Maximum rates at which the 7929 can execute Read Direct or Write Direct operations are:

60,000 operations/second in mode 1 or
110,000 operations/second in mode 2

PROGRAMMING

Standard Sigma input/output instructions (SIO, HIO, TIO, TDV and AIO) are used in programming the Model 7929. Eight toggle switches on the 7929 determine its device address, which the I/O instructions must use when communicating with that unit.

Status response returned during execution of SIO, TIO, and HIO is as follows:

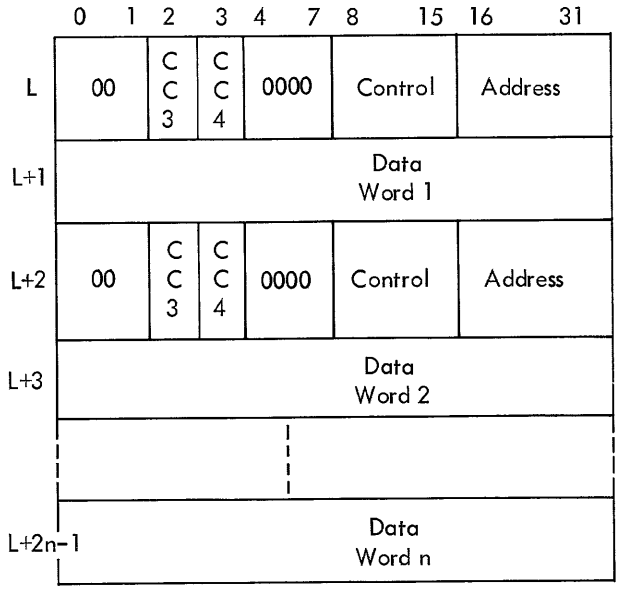
- Interrupt is pending from 7929.
- 7929 is either ready or busy.
- The last input or output operation was terminated because of unusual conditions.
- The 7929 recognized the program-specified device address.
- The 7929 can accept an SIO instruction (TIO only).
- The SIO instruction was executed successfully (SIO only).
- The 7929 was busy when HIO was executed (HIO only).

The TDV instruction enables the program to determine (1) whether a rate error has occurred, (2) the status response currently stored within the 7929, and (3) certain other diagnostic information.

Status returned during execution of the AIO instruction allows the reason for interrupt (rate overrun or other unusual conditions) to be determined.

In mode 1, the first byte the 7929 transfers to memory after receiving the Write Order is the status setting from the previous operation list. The next three bytes in sequence consist of one control byte and two address bytes, followed by four data bytes that form the 32-bit data word to be transferred. Bits 2 and 3 of the next sequential location contain the status conditions returned during the previous operation. This sequence of 8 bytes (one control, two address, four data, and one status) is repeated a program-specified number of times, depending on the number of RD or WD operations to be performed.

Each list in memory will appear as follows when operating in mode 1:

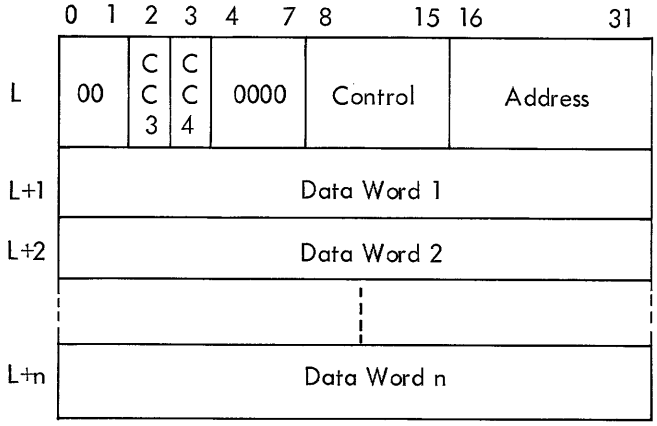


CC3, CC4 are status conditions returned by external device, corresponding to information that would normally be returned to condition code bits 3 and 4 in Sigma 7 when RD or WD was executed.

NOTE: Bits 2 and 3 of location L contain status conditions returned during the last operation of the previous list. Settings received for Data Word n are stored in the first byte location of the subsequent list.

In mode 2, the first four bytes transferred are identical to those in mode 1. The next 4n byte locations contain data words to be transferred; n depends on the number of RD or WD operations to be executed. Only the condition code setting received for Data Word n is stored. It is stored in bits 2 and 3 of the first byte location of a list associated with the next operation.

Each list in memory must appear as follows when operating in mode 2:



NOTE: Bits 2 and 3 of location L contain condition code settings returned during the last operation of the previous list. Settings received for Data Word n are stored in the first byte location of the subsequent list.

The format of the control and condition code bytes follow:

Bits 8-15 Control

Bit 8

A "zero" causes Read Direct operation to be executed.

A "one" causes Write Direct operation to be executed.

Bit 9

A "zero" causes the unit to operate in mode 1. (Each word pair contained in a list in main memory corresponds to a Read Direct or a Write Direct instruction.)

A "one" causes the unit to operate in mode 2. (The control byte and effective address of the first word in the list specify the operation and address to be used for all remaining data in the list.)

Bit 10

A "zero" causes the unit to operate at maximum rate permitted by interaction of I/O systems, the 7929, and external equipment.

A "one" causes the unit to operate under rate control of an external signal.

Bit 11

If set, enables an interrupt to be generated if the DIOA CC3 line is true during data transfer.

Bit 12

Same as 11 but for the CC4 DIOA line

Bits 13-15

Unused

Bits 0-7

Bit 2

Returns status line 1 (CC3) from the previous operation.

Bit 3

Returns status line 2 (CC4) from the previous operation.

NOTE: Bits 2 and 3 contain condition code settings for previous Write Direct or Read Direct operation.

Bits 0, 1, 4, 5, 6, 7

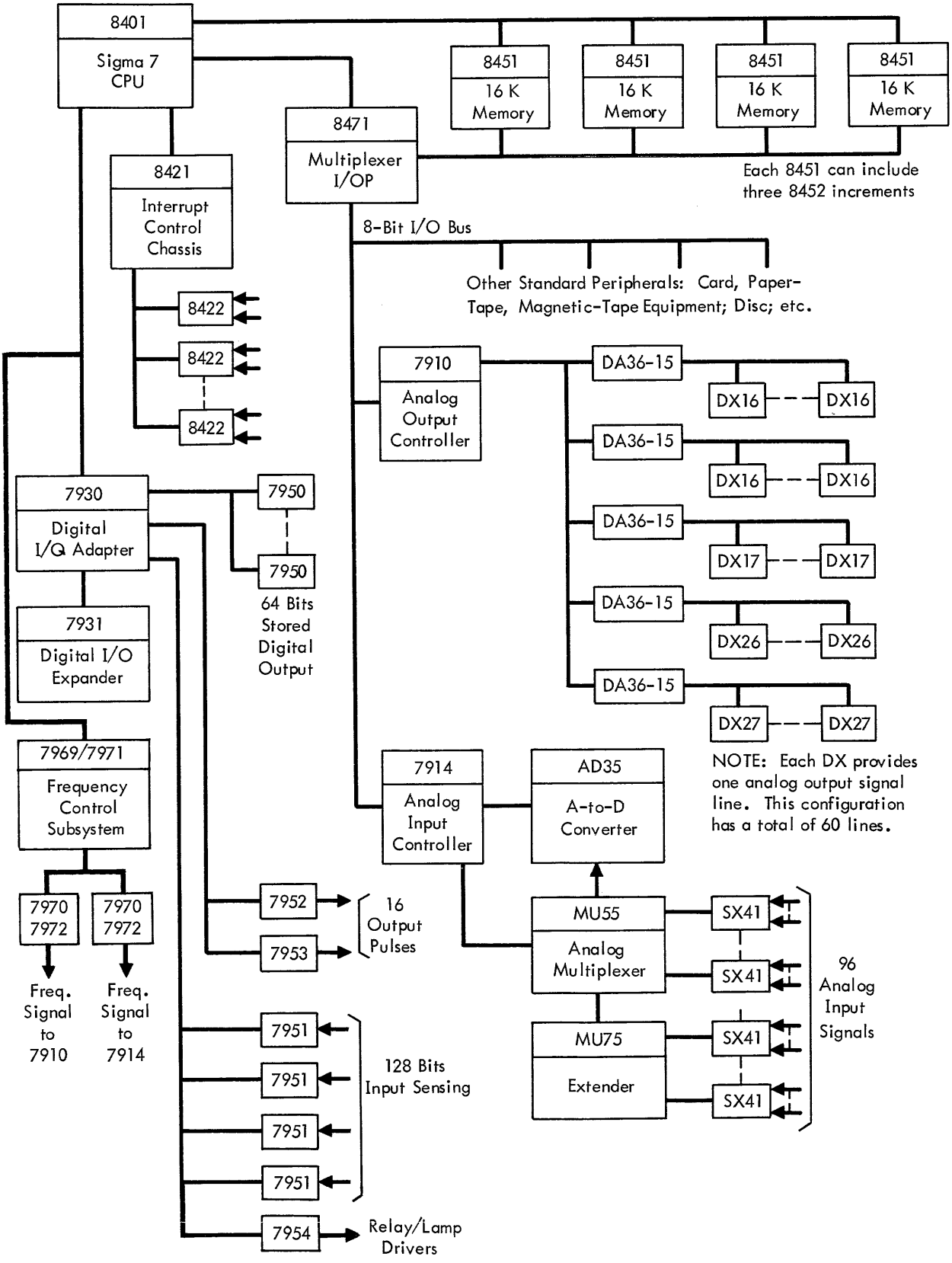
Unused

INTERFACE

Interface to the 7929 is identical to that of the direct input/output system, described in detail in SDS Publication No. 900973.

The 7929 provides four connectors for the DIOA interface, plus a fifth for external frequency control if needed. External devices attach to these connectors in a trunk-tail fashion, using shortest path length routing. These connectors provide the following signal lines:

- Address line 0 - Address line 15. 16 lines that carry the effective address during an RD or a WD operation.
- Data line 0 - Data line 31. 32 bidirectional lines used to transfer data during a RD or WD operation.
- Function Strobe. Generated by the 7929 during execution of an RD or WD instruction.
- Function Strobe Acknowledge. Returned to 7929 indicating address and function strobe recognition by a connected device.
- I/O Reset. Signal activated when I/O reset button on CPU console is depressed.
- WD/RD. Line that, when true, indicates current operation is Write Direct and, when false, Read direct.
- CC3, CC4. Status response lines supplied by external device.
- Clock. 1-Mc clock supplied to external device (50 percent duty cycle).



Typical Large Data Acquisition and Control System

Units that form the SDS Sigma digital input/output subsystem are manufactured by SDS as standard equipment to facilitate transfer of digital information between a Sigma computer and external devices. Under control of this subsystem, pulsed digital outputs, stored digital outputs, and digital inputs can be transferred economically and flexibly, and relays and lamps can be driven. These transfers allow the user to perform system control functions as well as data and status transfers.

DESCRIPTION

Here are the units that make up the subsystem:

Model No.	Item	
7930	Digital Input/Output Adapter	Control Units
7931	Digital Input/Output Expander	
7950	Stored Digital Output (8 bits)	I/O Function Modules*
7951	Digital Input Sensing (16 bits)	
7952	Pulsed Digital Output (8 bits; quiescent +8 volts)	
7953	Pulsed Digital Output (8 bits; quiescent 0 volts)	
7954	Latched Relay/Lamp Drivers (8 bits)	

Because these units may be combined in a completely modular fashion, the user need purchase (or lease) only those items necessary to implement his particular requirements. A significant cost savings can thus be realized both at the time of initial installation and during later expansion.

The Model 7930 Digital Input/Output Adapter connects directly to and is controlled by the direct input/output (DIO) interface of a Sigma computer. Up to eight 7930s can be attached to a single computer.

The Model 7930 is a basic control unit to which the hardware necessary to provide various types of stored digital outputs, pulsed outputs, and digital inputs can be added. I/O modules with model numbers of the form 795X can be installed in the 7930, in any sequence or mix desired, up to a total of 12 modules. Thus, one 7930 can provide for up to 96 output lines (stored type) or 192 input lines--or any mixture of functions in between.

*These modules plug into the control units.

The basic 7930 control unit can be expanded by adding one to three Model 7931 Digital I/O Expanders, each of which can accommodate an additional 16 I/O modules (from the 795X set). Hence, a fully expanded 7930/7931 subsystem can accommodate 60 I/O modules—the equivalent of 480 to 960 input/output lines (depending on types of I/O modules installed). A detailed description of the 795X I/O modules is presented at the end of this section.

A maximum allowable configuration for the digital I/O subsystem is shown in Figure 5.

OPERATION

Read Direct (RD) and Write Direct (WD) instructions control operation of the 7930/7931. During an RD instruction execution, the CPU presents a 16-bit address, accepts 32 bits* of data into a program-specified register, and indicates to the external device that an RD instruction is currently being executed. Information is transferred via the direct I/O bus.

During a WD instruction execution, the CPU presents a 16-bit address, transmits a 32-bit* data word from a program-specified register, and indicates to the external device that a WD instruction is currently being executed. Information transfer is via the direct I/O bus.

During the execution of an RD or WD instruction, the Model 7930 performs one of the following functions, as determined by the instruction being executed and its effective address:

1. If WD is being executed, one to four bytes (8 to 32 bits) in the unit can be loaded with the data word transferred from the CPU. The effective address of WD selects the I/O modules to be loaded. The output of each register is made available to connected external devices. In addition, a strobe is provided upon completion of data transfer to indicate to the external device that data is available in a particular holding register.

2. Alternatively, depending on the I/O module installed to correspond to a given WD address, output pulses (or relay/driving signals) can be generated. The effective address of WD determines the group. The state of corresponding bit positions in the data presented determines the pulses to be generated within the group. A "one" causes pulse generation. A "zero" causes no pulse generation.

*16 bits to accumulator in Sigma 2

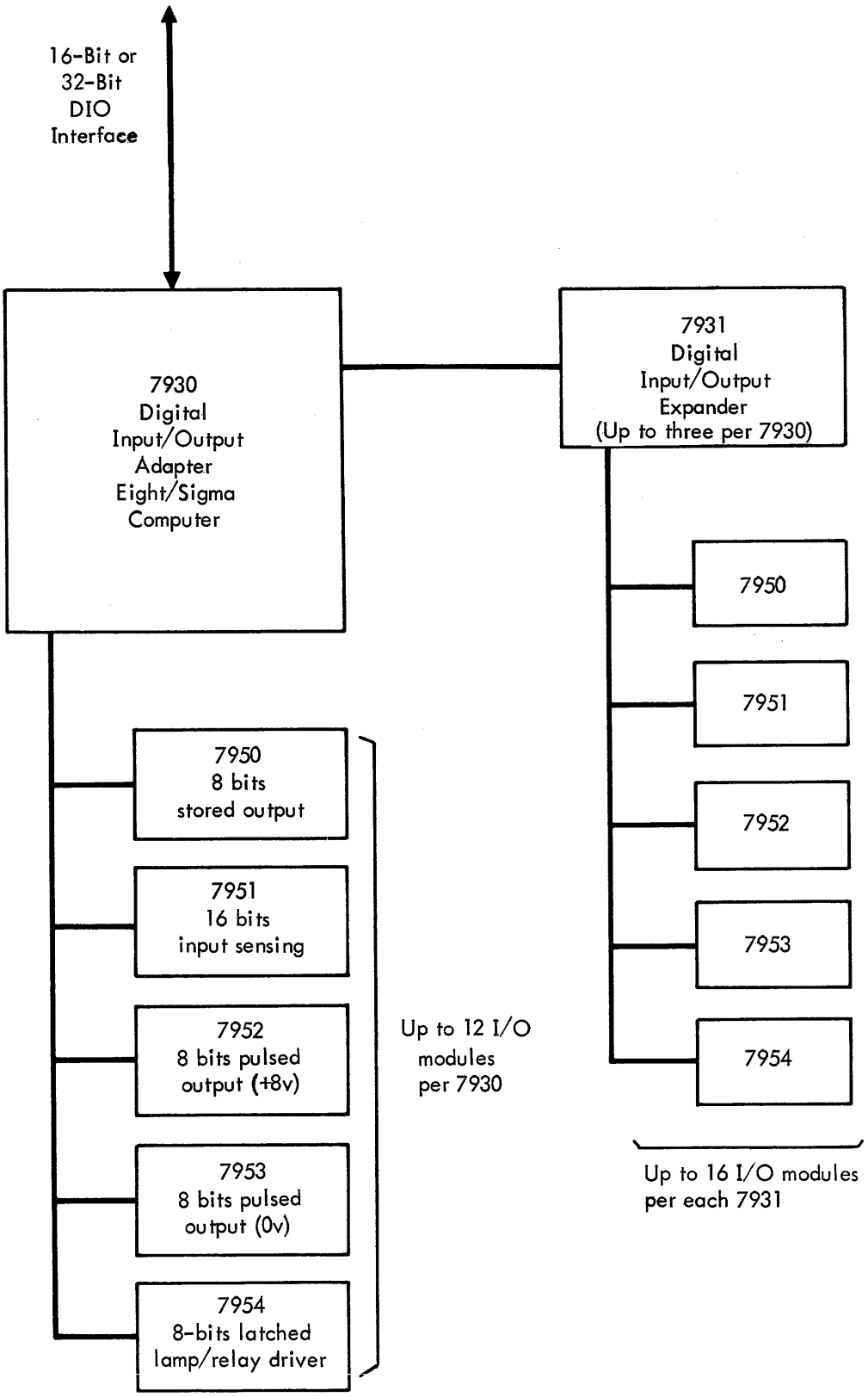


Figure 5. Interconnection Diagram, Digital Input/Output Subsystem

3. If RD is being executed, 16 or 32 input lines are selected for transfer to the program-specified register in the computer. The effective address of the RD selects the group and the bytes within the group.

PROGRAMMING

RD and WD instructions control the 7930 and 7931. The effective addresses of these instructions are interpreted as follows:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	1	0	0	U	U	U	S	G_0	G_1	G_2	G_3	B_0	B_1	B_2	B_3

The three bit positions designated "U" are for unit selection. They specify one of eight possible 7930/7931 subsystems.

S subselects "upper," or "lower" half of 16-bit I/O modules 7951).

G_0, G_1, G_2, and G_3 select one group of four I/O modules (out of a possible 15 groups) for control.

B_0, B_1, B_2, and B_3 select bytes (I/O modules) with the designated group. On Sigma 5 and Sigma 7, B_0 - B_3 = 1111 controls the entire group (32 bits). On Sigma 2, 0011 or 1100 must be used for maximum control (because of 16-bit data words).

WD instructions must be used to load the 7950 or 7954 or to control the 7952 or 7953. RD instructions must be used to read through the 7951.

Two additional features are:

- Feedback Control. Associated with I/O modules 7950, 7951, and 7954 is a feedback control line. If this line is grounded by an external unit, alteration of the associated I/O module is inhibited (when a WD is executed), and the status response bits CC3-4 (overflow/carry in Sigma 2) are set to "11."

- Pulse Duration. Switches within the 7930 can be set up so that output and strobe pulses have nominal durations of 1.0, 2.0, 3.0, or 4.0 μsec. Pulses can also be terminated any time within the preset period by means of a feedback signal from an external unit when using 7952s or 7953s.

Status response to RD/WD instructions (stored in CC3-4 on Sigma 5 or Sigma 7 or in overflow/carry indicators on Sigma 2) is as follows:

10 Input function I/O module

01 Output function I/O module

11 Operation rejected due to feedback control

00 Operation specifies I/O module address in which no I/O module has been installed.

INTERFACE

For transmission of signals between a 7930/7931 and external devices, 52-pin connectors are provided within the mounting case. Each connector accommodates the following signals:

- Four groups of eight data lines (can be input or output, depending on corresponding I/O module installed).

- Four strobe signals, one associated with each data byte of eight lines

- Four feedback control signals, one associated with each data byte of eight lines.

The interfaces of the various I/O modules (Models 795X) are described in the text that follows.

The Model 7950 Stored Digital Output contains eight dc latch circuits, each with transition-time limiters on the outputs (to reduce ringing and inductive coupling to other signal conductors). Switching time is 0.2 to 0.5 μsec. Output levels are ground (saturated transistor can sink 20 ma) and +8v through a 300-ohm resistor. The positive output level can be clamped by an externally supplied voltage to levels less than +8v if required.

Model 7951 Digital Inputs can receive digital input signals with one level at ground (must sink 4 ma) and the other level either floating (such as open contact) or +3 to +10v dc (negligible current).

Model 7952 and 7953 Pulsed Outputs have the same output circuit as the 7950.

The Model 7954 Relay/Lamp Driver contains eight dc latch circuits with high-current drivers on the output, which can switch 200 ma to ground from a load returned to up to +28v dc. The ground to which load current is switched must be wired to power ground externally as no connection to ground is made on the output circuit of the I/O module. For inductive loads, a clamp diode is available on the module to connect to a customer-supplied clamp voltage. For driving incandescent lamps, a "warm-up" resistor is available on the module.

The SDS Sigma Frequency Control Subsystem provides frequency control for SDS analog input, analog output, and digital transfer control units as well as for other devices not manufactured by SDS. The subsystem enables such units to perform operations at regular prespecified intervals selected manually or under program control.

DESCRIPTION

The subsystem consists of these units:

Model	Item
7969	Basic Frequency Unit
7970	Frequency Source Unit (Manual)
7971	Basic Program Control
7972	Frequency Source Unit (Programmable)

The Model 7969 Basic Frequency Unit is a control chassis that can house one 7971 and up to four 7970s or 7972s in any mixture. Two 7969s can be added to a single Sigma computer, allowing up to eight program-controlled external frequency sources in a fully expanded system.

The Frequency Source Units (7970 or 7972) generate 2-μsec pulses at intervals ranging from 5 μsec to 1.9 sec. For each 7970, eight toggle switches control this time interval in 1-μsec increments. A clock input of 640 kc (maximum) is provided automatically as part of the 7969.

The Model 7972 Frequency Source Unit (programmable) allows program selection of time interval. A Model 7971 is required before any 7972s can be added.

Figure 6 shows a frequency control subsystem in which output frequency is manually selected. Figure 7 shows a subsystem in which output frequency is programmable for frequency source units 1 and 3.

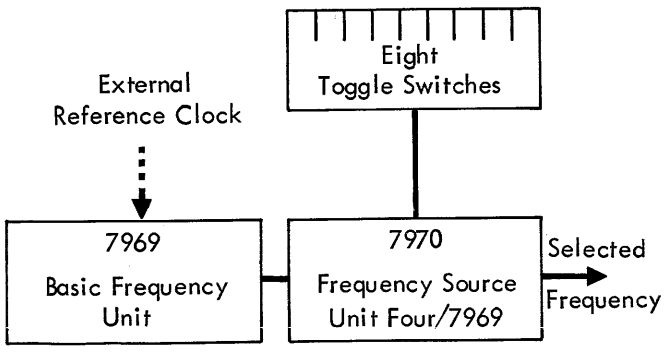


Figure 6. Frequency Control Subsystem with Manual Selection of Output Frequency

OPERATION

The required basic clock frequency is provided within the 7969 by a crystal-controlled oscillator at a selectable rate from 10 kc to 640 kc. Optionally, the 7969 can be driven by a user-supplied clock with a frequency of 1 Mc or less and minimum "on" or "off" times of 500 nsec. Resulting time intervals on the various 7970s or 7972s will then be increased by a factor proportional to the ratio of the external clock's period to 1 μsec.

For each 7970, the setting of eight toggle switches determines the frequency of occurrence of output pulses, represented mathematically by:

$$f = \frac{\text{basic clock frequency}}{(N + 1)}$$

where

N is the decimal equivalent of the binary configuration represented by the eight toggle-switch settings

and

$(4 \leq N \leq 255)$

When used with standard SDS units providing a 640 kc basic clock:

$f_{max} = 128$ kc

$f_{min} = 2500+$ cps

PROGRAMMING

For each 7972, a Write Direct (WD) instruction from the Sigma computer controls the output pulse frequency. During its execution, the central processor presents a 16-bit address and transmits a 32-bit data word from a program-specified register.

The 16-bit effective address of the WD instruction determines the 7972 selected for control according to the following table:

Unit No. 7972	First 7969	Second 7969
0	X'A000'	X'A004'
1	X'A001'	X'A005'
2	X'A002'	X'A006'
3	X'A003'	X'A007'

The low-order 12 bits of the data word transmitted during the execution of the WD instruction specify the frequency selected for the addressed 7972, represented mathematically as follows:

$$f = \frac{\text{basic clock frequency}}{(N+1)}$$

where

N is the decimal equivalent of the low-order 12 bits of the data word

and

$$4 \leq N \leq 4095$$

with a 640 kc basic clock:

$$f_{max} = 128 \text{ kc}$$

$$f_{min} = 156+ \text{ cps}$$

Further, the frequency control subsystem has two additional characteristics: (1) each clock output can be individually turned on or off under program control (when 7972 is installed) and (2) the programmer can direct that an output pulse be generated coincident with the execution of the Write Direct instruction, which transmits the frequency data word to the 7972.

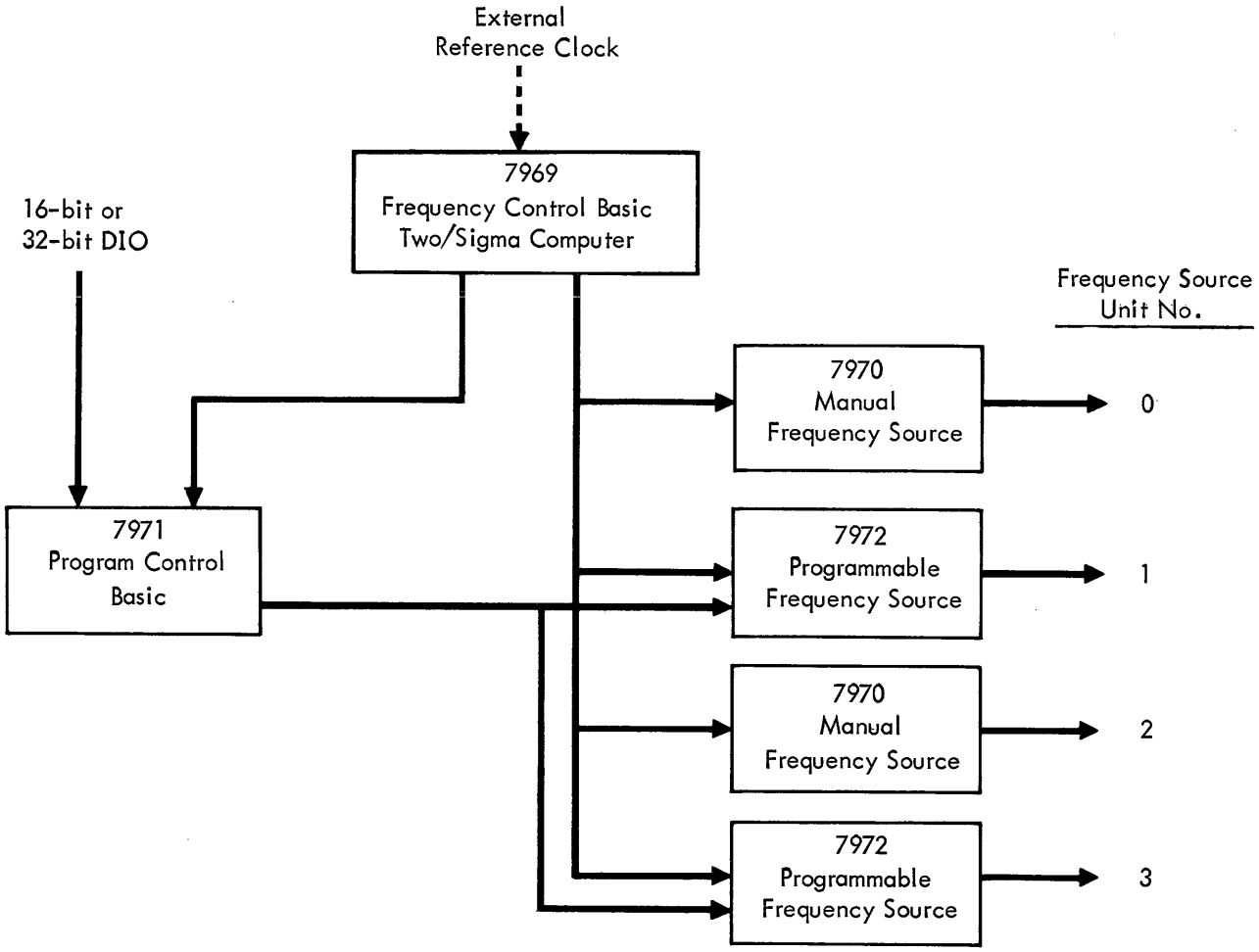


Figure 7. Typical Frequency Control Subsystem with Mixed Manual and Program Selection of Output Frequency

SDS MODEL 7900 DEVICE SUBCONTROLLER

The SDS Model 7900 Device Subcontroller provides a means for standardizing certain common parts of device controllers* that, in turn, connect a customer's device or signals to the 8-bit input/output interface channel on a Sigma computer. It permits quicker design and check-out of custom-designed equipment and improves maintainability (thus reducing equipment "down-time"). The Model 7900 provides, in a standard fashion, certain common functions that must be present in all equipment attached to the 8-bit Sigma interface. This subcontroller is an integral part of almost all SDS standard Sigma peripheral controllers.

DESCRIPTION

As shipped to a customer, the Model 7900 comprises a standard Sigma T Series card cage that —

1. Mounts in 19-inch rack.

2. Occupies approximately 5-1/4 inches of vertical rack space with a depth of approximately 6 inches.

3. Includes a ground plane, which provides for attaching power wiring.

4. Includes 32 SDS standard 52-pin bifurcated, gold-plated wire-wrap connectors, designed to accept standard T Series modules (described in SDS brochure 64-51-03R).

Ten of these connectors are wired to implement the logic of the device subcontroller, and nine modules (one is double-size) are tested and installed in those slots before shipment. The remaining 22 connector positions are available to facilitate design of the customer's special logic: wiring connections can be made on the back panel to the subcontroller as required. If a customer's device controller requires more space than the available 22 slots provide, additional T Series card cages can be purchased and mounted vertically adjacent to the 7900. Cross-chassis back-panel wiring can be added as required.

At the time of purchase of the Model 7900, fixed mounting, left hinge, or right hinge can be specified. Overall listed mounting dimensions remain applicable.

DETAILED FUNCTIONS

The Model 7900 unit is the standard means of connecting to the Sigma 8-bit I/O system. When various "rules" governing interfacing to this unit are observed, the device subcontroller ensures maximum input/output data transfer rates for a Sigma system, subject to delays introduced by long cables.

Functions performed by the 7900 include the following:

1. Provision is made for cable* connections. Cables that connect to four of the modules in the 7900 assure that electrical and logical connections to the 8-bit I/O interface are properly made. No additional space is required for connecting to the I/O system.

2. Each device controller in a system must respond to only one particular I/O address generated by the Sigma CPU. Eight switches on the 7900 permit selecting this address for each controller based on the particular installation requirements. The switch outputs are available, as is a signal that indicates a "match" between the switch states and the CPU's address lines. This same address is transmitted to the CPU to acknowledge peripheral interrupts and to permit the I/O system to service this controller.

3. A switch in the 7900 controls a pair of relays that allow the entire controller to be logically and electrically disconnected from the I/O system. Thus, the unit can be switched off-line for test or maintenance purposes without removing cables or disrupting operation of the remainder of the system. If power to this controller fails, the unit is also switched off-line, which prevents a power failure in one unit from interfering with proper system operation.

4. Each Sigma system device controller is assigned a hard-wired priority for acknowledging interrupts by peripheral devices and for servicing by the I/O system. The 7900 automatically determines the priority, in response to various CPU stimuli, and provides a signal to be used in controller design that denotes when this unit is to become active for data transfers or interrupt acknowledgement.

5. Device controllers usually must provide various types of status response information when "queried" by the CPU or I/O system. The subcontroller automatically gates the proper status bits onto the proper data lines at the right time for the correct duration as required by the I/O system.

6. The Model 7900 contains five control flip-flops that eliminate certain improper conditions which might otherwise occur at the interface to impair or prevent its proper operation. These conditions could possibly endanger the integrity of the entire I/O system. A signal provided to the controller by one flip-flop exactly defines that period of time during which data transfers can take place between each device controller and the I/O system.

*"Device controller" is the name SDS gives to the control unit that interfaces between the Sigma 8-bit I/O interface and any external device or set of external signals.

*Must be purchased separately in the required lengths.

SDS standard software for system interface units is organized into three distinct groups: (1) maintenance and calibration routines, (2) device control routines (handlers), and (3) service (data manipulation) routines. In each case, the programs are compatible with software for all standard SDS products.

MAINTENANCE/CALIBRATION ROUTINES

All SIU maintenance software is controlled by the SDS Sigma Diagnostic Control Program (DCP). The DCP enables the user to control calibration or maintenance functions with a Syntactical Test Language. The user can combine primitive diagnostic functions to form a complex maintenance test that will operate without further operator intervention for an extended period of time.

Test parameters are defined as static directives. Each parameter can be modified individually, thus eliminating the need for extensive type-in to change one parameter during a maintenance test. Complete maintenance tests are provided with predefined static parameters. Therefore the user can perform a series of routine maintenance tests with a minimum of typewriter communication. If problems develop, the user can dynamically change the static parameters to facilitate system maintenance.

7910/7914 Maintenance Program Package

This program package contains a group of static directives (parameters) and active directives (maintenance tests) that provide a convenient method of testing, adjusting, and demonstrating the operation of the standard analog input and output units. Table 2 lists the directives for this package.

The passive directives have the default values shown in parentheses in Table 2. These values can be changed by the operator prior to or during the test.

The active directives are discussed individually below.

Single-Value Output (7910). This test allows the user to set the scope D-to-A converter to a desired voltage.

Sweep Test (7910). A sawtoothed waveform is continuously generated for display on the specified D-to-A converter. The user then observes the converter's operation and linearity on an oscilloscope.

Single-Channel Input (7914). When a fixed voltage is applied to a multiplexer input, the program samples the voltage on one input channel, computes the mean and standard deviation over n samples, and prints a histogram of the samples. The statistical description of the variance provides the user with a measure of the noise on the channel.

Table 2. Directives for 7910/7914 Maintenance Program Package

Passive Directives*	
ADL	A-to-D converter length in bits (12)
DAL	D-to-A converter length in bits (9)
ADV	A-to-D converter full-scale voltage (10v)
DAV	D-to-A converter full-scale voltage (10v)
NS	Number of samples for SCI, SIT, CLC, CLH (1000)
AID	Input device controller address (0)
AOD	Output device controller address and channel address (011)
ADD	Display device controller address and channel address (011)
ADF	A-to-D converter frequency (external control, no frequency control)
DAF	D-to-A converter frequency (external control, no frequency control)
Active Directives†	
SVO	Single-value output to D-to-A converter (7910)
ST	Sweep test (7910)
SCI	Single-channel input (7914)
SIT	Summary input test (7914)
CLC	Closed-loop calibration (7910/7914)
CLH	Closed-loop histogram (7910/7914)

*Default values are in parentheses
†Maintenance tests

Summary Input Test (7914). This test allows the user to verify the accuracy of a number of multiplexer channels in a short period of time while operating the equipment in a user-specified mode. The selectable modes include random, sequential, or same-channel selection, with or without external frequency control.

Closed-Loop Calibration (7910/7914). This program allows the user to calibrate the analog inputs by the use of analog outputs connected to the analog inputs and an oscilloscope display.

Closed-Loop Histogram (7910/7914). This program allows the user to test both analog outputs and inputs concurrently over their common range with a large number of random values. Results are given in the form of mean error, standard deviation, and an optional histogram. The statistical variance provides a test of noise and linearity over the total range.

7930 Maintenance Program Package

This program package provides a convenient method of testing and demonstrating the standard digital input and output units. Table 3 lists the available directives for this package.

Table 3. Directives for 7930 Maintenance Program Package

Passive Directives*	
CONT	7929 controller presence/absence
DO	Digital outputs 7930 number (0)
DI	Digital input 7930 number (0)
POL	Pulsed output location (101)
SOL	Stored output location (101)
DIL	Digital input location (101)
Active Directives†	
POT	Pulsed output test (7952/7953)
SOT	Stored output test (7950)
DIT	Digital input test (7951)
CLT	Closed loop test (7950/7951)

*Default values are in parentheses
†Maintenance tests

The active directives for the 7930 Maintenance Program Package are discussed individually below.

Pulsed-Output Test (7952/7953). This test allows the user to verify, with the aid of an oscilloscope, the proper functioning of the 7952/7953 system interface units.

Stored-Output Test (7950). This program allows the user to change the state of the stored outputs according to a specified pattern and to verify the specified pattern on an oscilloscope.

Digital-Input Test (7951). This program allows the user to check out the digital input modules since the program lists the status of the 7951.

Closed-Loop Test (7950/7951). With this program, the user can automatically test the stored output and input capabilities of the system. The test assumes that one of the output (7950) groups has been connected to one of the input (7951) groups by the closed-loop cable, which is provided with the hardware. Optionally, the user can elect to "close the loop" between digital inputs and outputs at a remote system patch panel, checking the entire data transmission path.

7922 Maintenance Program Package

This program package provides a convenient method of testing, adjusting, and demonstrating both standard analog input/output and digital input/output under control of the Model 7922 Analog and Digital Adapter. This package contains all of the directives described in the 7910/7914 and 7930 packages, except for the 7929 passive directive "CONT." However, the directives in the 7922 package are distinguished by the character X following the active directives and all 7930-type passive directives. For example:

DOX	POTX
DILX	ADL
CLTX	DAF

The parameters of the 7922 directives are identical to those of the 7910/7914 and 7930 directives. The functions performed by these directives are identical.

DEVICE CONTROL ROUTINES (HANDLERS)

These I/O handlers provide a complete and easy-to-use means for user programs to control the operation of the 7914 Analog Input Controller, 7910 Analog Output Controller, 7922 Analog and Digital Adapter, 7969 Frequency Control Subsystem, and 7930 Digital I/O Subsystem.

System Generation

SIU handlers receive certain parametric information from the SYSGEN program, including equipment configuration, controller addresses, presence of various options, interrupt level assignments, etc. For stand-alone use, these parameters are assembled with the stand-alone handlers.

Control Information

The SIU I/O handler is designed to operate the analog front-end portion of the system at the maximum equipment rates. Toward this end, maximum control is afforded the user who wants it. Input/output is controlled by three types of information: (1) Data Control Block (DCB), (2) Buffer Command Data (BCD), and (3) Command List (CL). These three sources of control information must be generated at assembly or compiler time to obtain maximum throughput rates. Run-time generation of DCB, BCD, or CL tables is permitted; but this procedure usually results in throughput degradation. Each source of information is discussed in applicable reference manuals for the SDS stand-alone or monitor systems used on the various Sigma computers.

Applications

The user can use the I/O handlers at various speeds to solve a complete range of problems. Some typical applications are discussed below. In these examples, it is assumed that the DCB, BCD, and CL tables are constructed.

Simple Analog Input. The handler used for simple analog input is:

```
CALL ANALOG (DCB)
```

This call scans n channels of analog input information according to the buffer command data. There are three primary modes of use:

- Random scan: Random mode with a multiplexer channel address for each data point.
- Complete scan: Automatic mode with every channel scanned sequentially until the byte count is zero. If the byte count is greater than the count required to scan all the channels, the scan continues recycling.
- Partial scan: Automatic mode with a continuous subset of the channels scanned. Same as complete scan but with an analog multiplexer address and a subset of the total number of channels defined.

Buffered Analog Input. This mode is a continual scan of the channels until a termination order is given by a CALL TERM statement. The first statement issued is a CALL ANALOG (DCB) with the indefinite flag set in the DCB. This call starts an indefinite scanning sequence controlled by command chaining in Sigma 5 and Sigma 7 and by data chaining in Sigma 2. I/O interrupts are generated at the end of each record. A typical program is:

```
[LOOP] CALL ANALOG (DCB) ◄—A buffer full return.

Process A buffer (may be I/O to disc or tape)

CALL ANALOG (DCB) ◄— B buffer full return

Process B buffer

go to [LOOP] until done

CALL TERM (DCB)
```

Return to the program is made after each buffer is filled. This process is continued until the I/O is terminated.

Analog Output. The output handler is the same as the input handler except that DCB control information specifies "write" instead of "read." The control information is contained in the DCB, BCD, and CL tables. The BCD information is equivalent to the random-mode operation for the input handler.

The calling sequence for simple output is:

```
CALL ANALOG (DCB)
```

The sequence for buffered output is:

```
[LOOP] CALL ANALOG (DCB) ◄—A buffer empty return

Process A buffer (read new data from disc or tape possibly)

CALL ANALOG (DCB) ◄—B buffer empty return

Process B buffer

go to [LOOP] until done

CALL TERM (DCB)
```

Return to the program is made after each buffer is output. This process is continued until the I/O is terminated.

Digital Input/Output (DIO). The DIO handler provides the capability to transfer pulsed digital outputs, stored digital outputs, and digital inputs easily and flexibly. The Data Control Block contains the following information relative to the DIO:

Data buffer address
Error return address
Device address
Number of bytes to transfer

Digital input/output will be in one of the following two modes:

- Mode 1, in which a new control byte and 16-bit address are supplied for each data word transfer.
- Mode 2, in which the first control byte and 16-bit address apply to all remaining data (i.e., multiple words are being delivered to or received from a single external device).

I/O operation is called as follows:

CALL DIO (DCB)

The Mode 1 data is input/output with a different WD statement for every 32 bits (for Sigma 5 and 7) or 16 bits (for Sigma 2) until all data words have been input/output. The Mode 2 data is input/output to the same group of lines with only one RD/WD instruction. In both cases the handler performs the end action and error checking before returning to the user program.

7922 I/O Handler. The 7922 handler provides control for both analog and digital I/O. Data rates with this device are slower than for the 7910, 7914, 7930, etc.; and the handlers reflect this in their design.

When the 7922 handler is performing digital I/O, its format and operation are the same as for digital I/O through the 7930 except for the effective address.

When the 7922 handler is performing analog I/O, its format and operation are the same as for analog I/O through the 7910 and 7914 except that (1) effective addresses are different and (2) a calling-routine option is available in the 7922 handler to allow analog input in either an interrupt-control mode or a "locked" mode (i.e., "stall" on conversions).

7929 I/O Handler. The 7929 handler allows a 7922 or a 7930 to operate on a Sigma Multiplexor IOP (MIOP) channel. The data format is the same as for the 7922 or 7930 and the operation is the same from a user's program. However, the handler creates a command word to perform I/O through the MIOP.

7971 I/O Handler. The frequency control function (FREQ) permits the user to set the 7972 Frequency Source Units to any allowable value. A typical FORTRAN call might appear as follows:

CALL WRITE (DCB)

where the DCB arguments are as follows:

Device address
Frequency value
Error return

SERVICE (DATA MANIPULATION) ROUTINES

Service routines fall into three major categories--DCB, CL, and BCD--based on the type of structured table they generate.

They are further subdivided into (1) assemble/compile-time service routines and (2) execution-time service routines. Either the assemble/compile-time or the execution-time routines can be used for creation of DCB, CL, and BCD tables. In addition, the execution-time service routines can be used to convert partial fixed-point words to full fixed-point words (or vice versa).

Table 4. Installation Data

Name of Unit	Physical Description	Where Installed	Internal Cabling to Sigma*	SIU to Device Cabling†
Analog Input Controller (7914)	One chassis‡	Sigma I/O cabinet, any chassis position	Four cables to 8-bit I/O system bus (Model ET10)	One ET20 from 7914 to A-to-D converter; one ET21 from 7914 to multiplexer
Analog Output Controller (7910)	One chassis	Sigma I/O cabinet, any chassis position	Four cables to 8-bit I/O system bus (Model ET10)	Two ET10s from 7910 to first DA35 or DA36; two ET10s from each DA35 or 36 to next DA35 or 36
Analog and Digital Adapter (7922)	One chassis	Sigma I/O cabinet, any chassis position	Three cables to Sigma direct I/O bus (Model ET10)	Same as 7910 and 7914 for analog instruments; similar to 7930/31 for digital signals
IOP-to-DIO Adapter (7929)	One chassis	Sigma I/O cabinet, any chassis position	Four cables to 8-bit I/O system bus (Model ET10)	Four ET10s to external devices(s), plus one ET10 to 7970/7972 or other frequency source.
Digital I/O Subsystem (7930, 7931, 7950, 7951, 7952, 7953, 7954)	7930, 7931: one chassis each. 7950, 7951, 7952, 7953, 7954: one module each	7930s and 7931s each occupy a single chassis position in a Sigma I/O cabinet. 7950, 7951, 7952, 7953, and 7954 plug into 7930 or 7931 as required	7930: four cables to Sigma direct I/O bus or to 7929 bus (Model ET10)†† 7931: two cables to 7930 7950, 7951, 7952, 7953, 7954: none	Customer-fabricated cables using ZT15 cable plug modules or ET10 cables to each I/O Module
Frequency Control Subsystem (7969, 7970, 7971, 7972)	7969: one control chassis; accommodates one 7971 and four 7970s or 7972s	7969 occupies one chassis position in a Sigma I/O cabinet. 7970, 7971, and 7972 plug into 7969 as required	7969/7970/7972: none 7971: three cables to Sigma direct I/O bus (Model ET10)††	One ET10 from each destination to next destination

*Cables listed in this column are provided free as part of normal unit installation,

†Cables between these system interface units and terminal devices must be purchased separately.

‡Chassis are standard SDS 32-module card cages.

††Three cables only for Sigma 2.

SDS SCIENTIFIC DATA SYSTEMS • 1649 Seventeenth Street • Santa Monica, California 90404

Printed in U.S.A. 64-28-01B (Rev. 2)